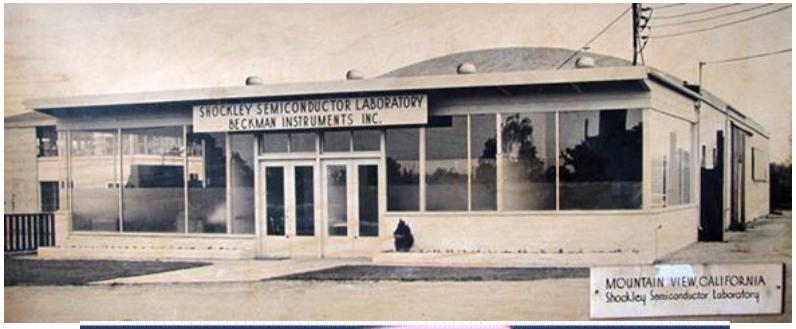
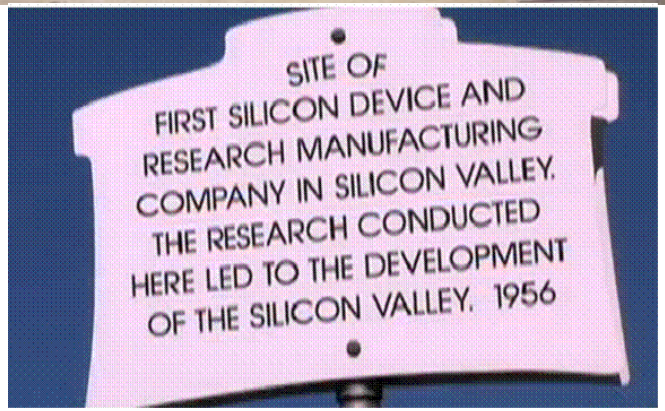
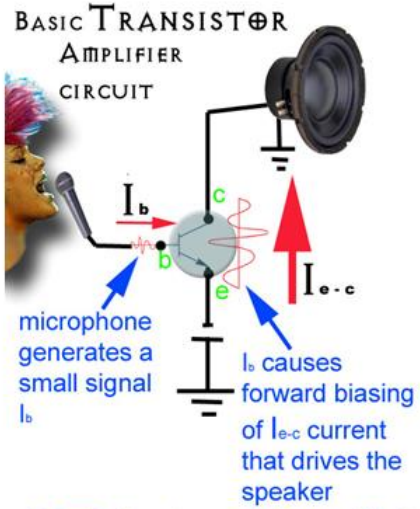
Silicon Technology

The Invention of Transistor (1947)



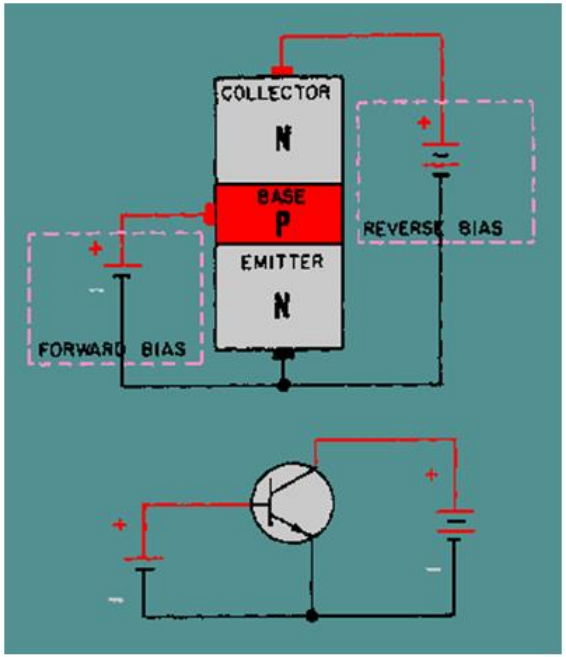


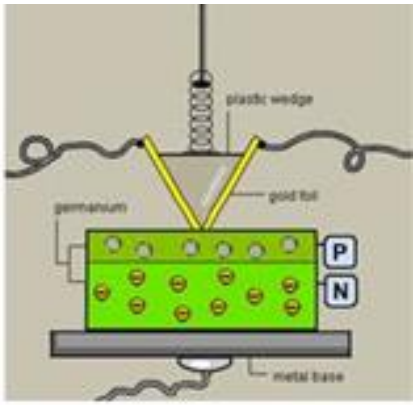
Shockley Semiconductor at 391 San Antonio Road, Mountain View, Santa Clara County (Chemical Heritage Foundation).



NOTE: the shape of the amplified wave is the same shape as the signal but has greater amplitude

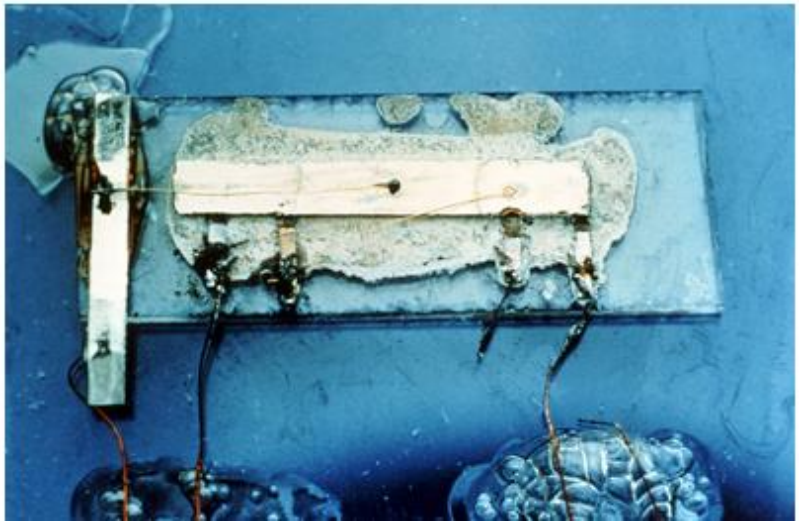
amplification = I_{e-c} / I_b

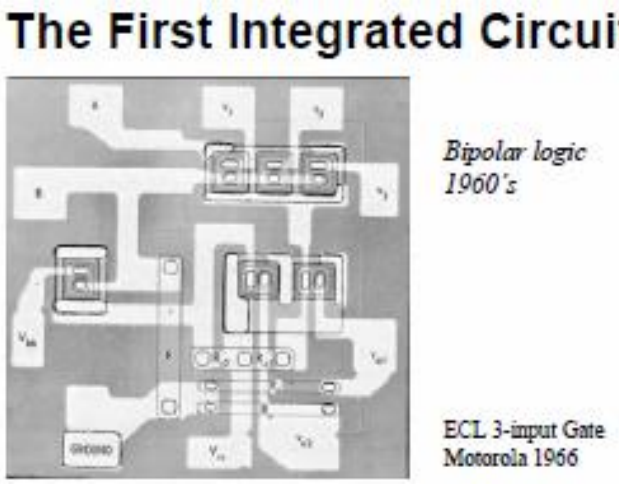




The Invention of the Integrated Circuits (1958)

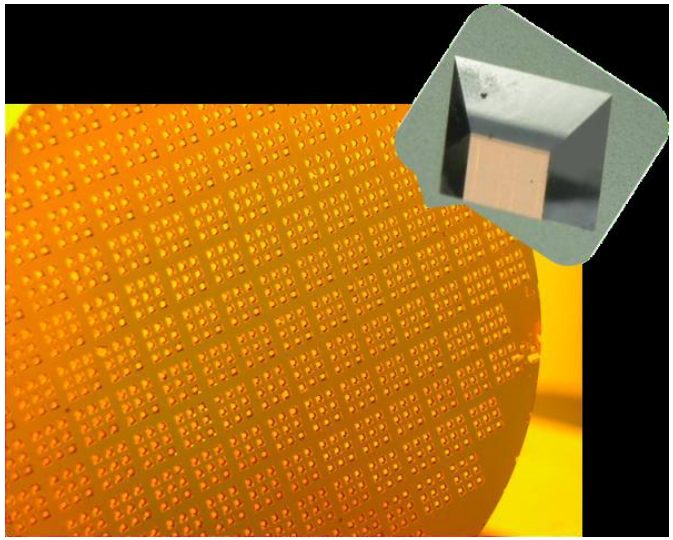
(Jack Kilby & Robert Noyce)





The Discovery of Piezoresistive Effect (1954)

- **Discovered by C.S. Smith**
- **The piezoresistive effect of semiconductor can be several magnitudes larger than that in metals.**
- **Many MEMS devices such as strain gauges, pressure sensors, and accelerometers utilize the piezoresistive effect in silicon.**



An Example of a Piezoresistive Pressure Sensor
[MTTC Pressure Sensor]

Sandia National Laboratory

Chemical Vapor Depositions for MEMS

Nang Tran (Univ. of Minnesota, USA)

- **Part 1: What is MEMS technology?**
- **Part 2: Chemical vapor deposition techniques (CVD) for MEMS**

CVD Plays a Pivotal Role both in VLSI and MEMS

VLSI

1. Focus on electrons
2. No moving part
3. Two dimensional
4. Electrical systems
5. Si, Ge, dielectrics used
6. IC isolated from surroundings

MEMS

1. Focus on mass
2. Various moving parts: micro gears, valves, pumps
3. Three dimensional structures
4. Electric, mechanical, chemical, biological systems
5. Si, oxides, polymers, plastics used
6. Interaction with environment

First wave: Only a couple of companies can afford the next technology evolutions

IC + MEMS =

THE SECOND WAVE: RE-USE OF SEMICONDUCTOR PROCESS TO MAKE NON IC DEVICES IS CREATING TOTALLY NEW OPPORTUNITIES.

What is MEMS Technology?

1. **Introduction to MEMS**
2. Common materials in MEMS
3. Etching
4. Surface micromachining
5. Bulk micromachining
6. Molding

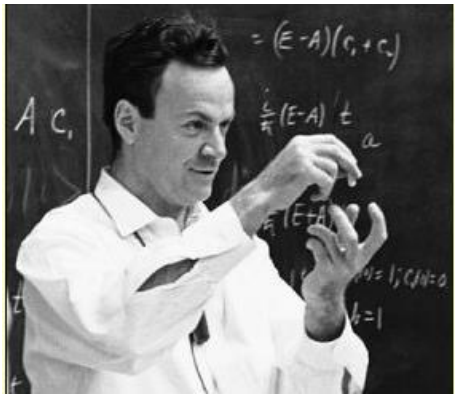
Feynman's Dream

1959: Richard Feynman dreamed big (Oops, small!)

- Richard Feyman offered a prize to challenge those who could build a motor of only 1/64 inch cube (1959).
- Bill McLellan successfully built a 2000 rpm motor, 250 μg, 13 parts by hands with tweezers and a microscope (1960).

"There is plenty of room at the bottom"

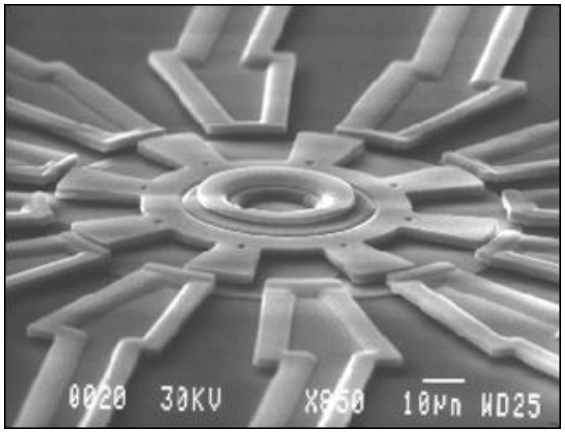
Why can't we write the entire 24 volumes of Encyclopedia Brittanica on the head of a pin?

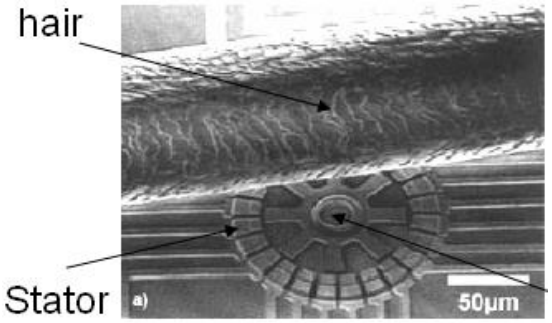


Polysilicon as a Mechanical Material

(The first rotary drive motors, 1988)

- **Invented by Dr. Muller and Dr. Howe of UC Berkeley**
- **Established sacrificial etching process using : (i) polysilicon as a mechanical structure material and (ii) oxide as a sacrificial material.**





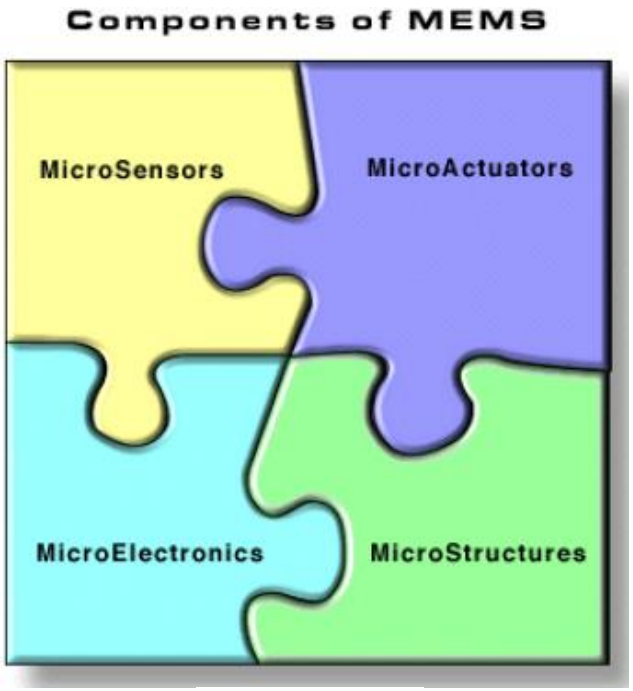
First Rotary Electrostatic Side Drive Motor
[Richard Muller, UC Berkeley]

The Dream Has Become a Reality

Microsensors: pressure, position, speed, acceleration, temperature, flow and various optical, chemical, environmental, and biological variables.

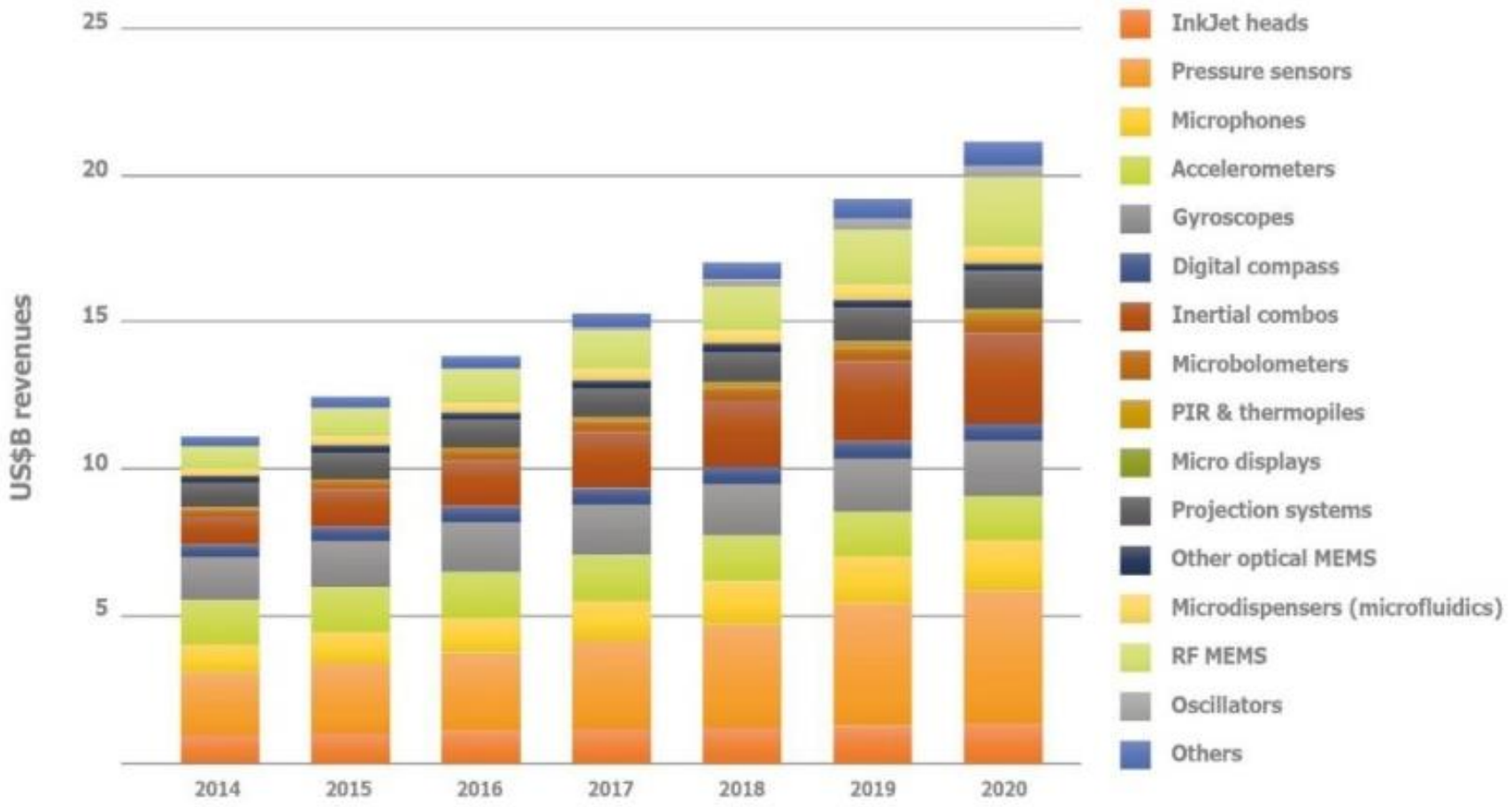
Microstructures: microscopic lenses, mirrors, nozzles, gears and beams.

Microelectronics: ink-jet printing heads, magnetic heads, compact disks, medical applications, automotive components, chemical and environmental applications



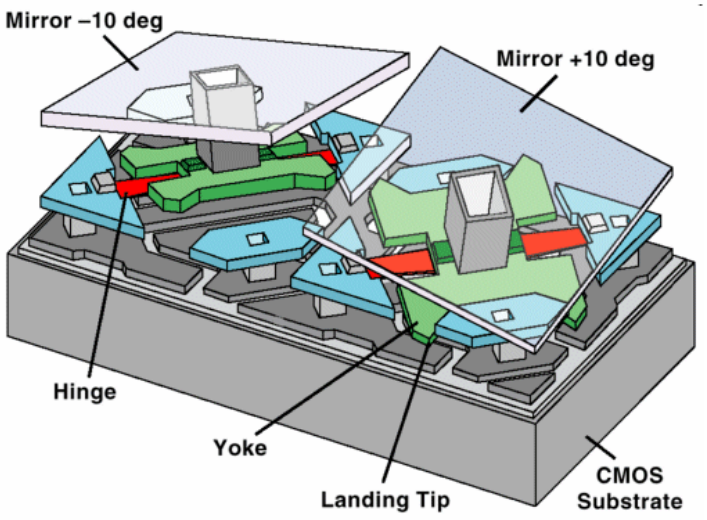
Microactuators: valves, switches, pumps, rotational and linear motors.

MEMS Market Can Reach $22B in 2020 (FromYole Development)

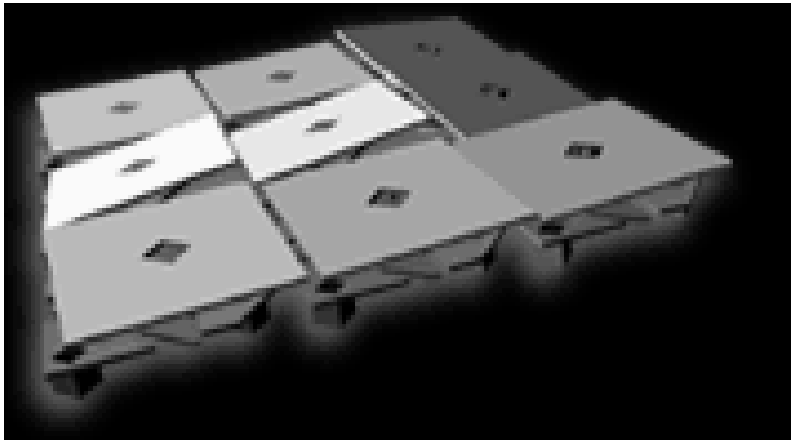


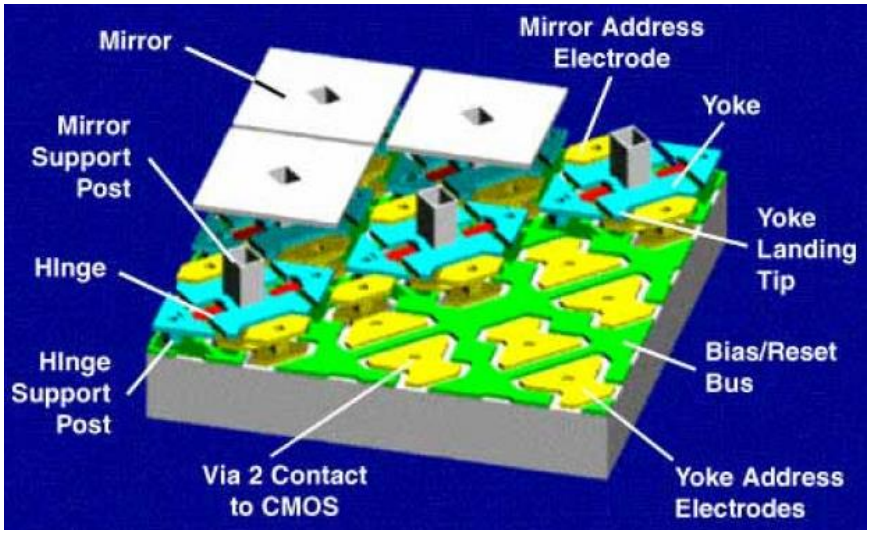
Digital Micro-mirror Device (Larry Hornbeck, TI,1994)

- Array of up to 1.3 million mirrors
- Each mirror is 16 μm on a side with a pitch of 17 μm
- Resolutions : 800x600 pixels and 1,280x 1,024 pixels
- Mirror is moved by 24V applied
- Projection system consists of DMD, electronic light source and projection optics
- 16 μs switching time.



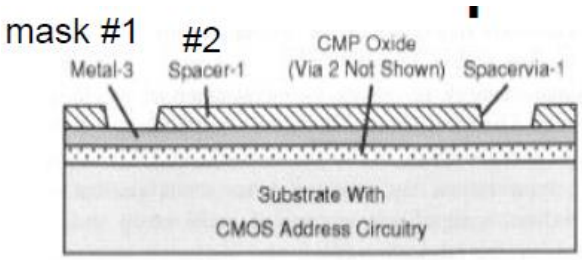
DMD Pixel (transparent mirror, rotated)





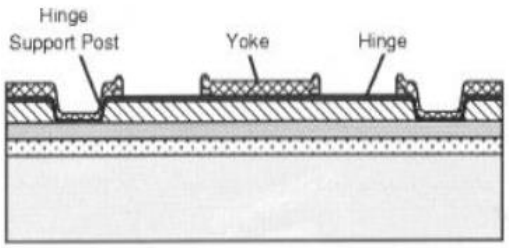
From "An Introduction to Microelectromechanical Systems Engineering" by Nadim Maluf

DMD Process Flow (Wagner/Meyners)



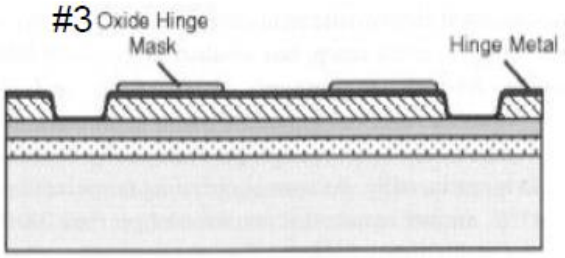
After Spacer-1 Patterning

Spacer 1 : Photoresist



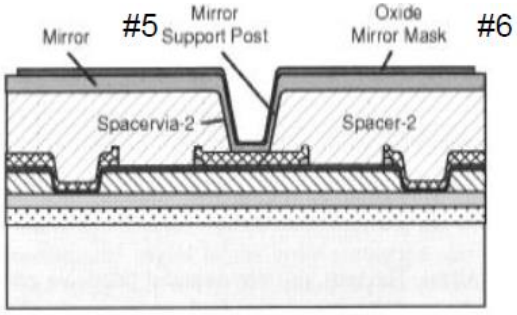
After Yoke/Hinge Etch and Oxide Strip

Oxide hinge mask: PECVD SiO_2



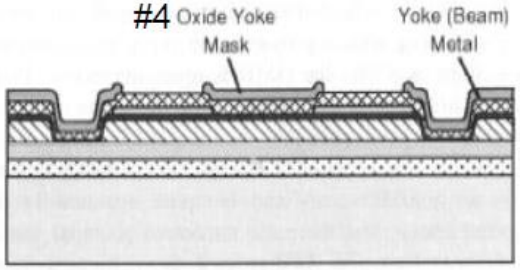
After Oxide Hinge Mask Patterning

Hinge metal : $Al_{98}Si_{1.0}Ti_{0.2}$ (60 nm)

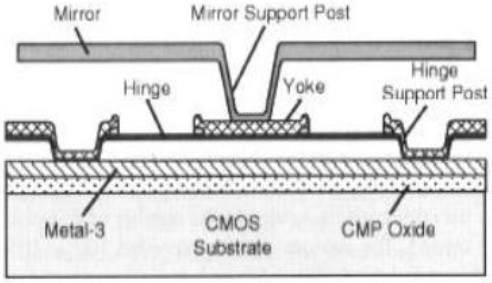


After Mirror Oxide Patterning

Yoke metal : Al

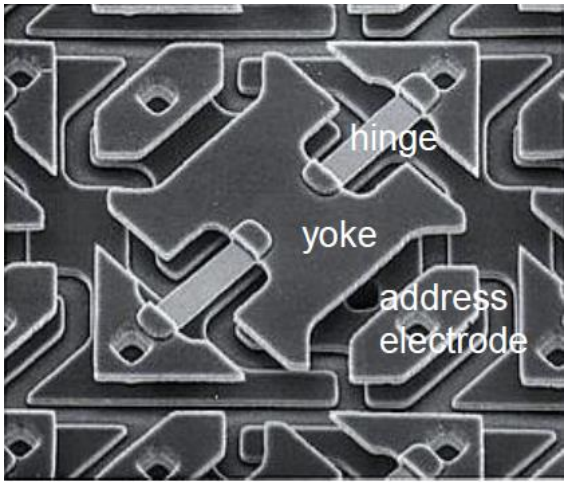


After Yoke Oxide Patterning

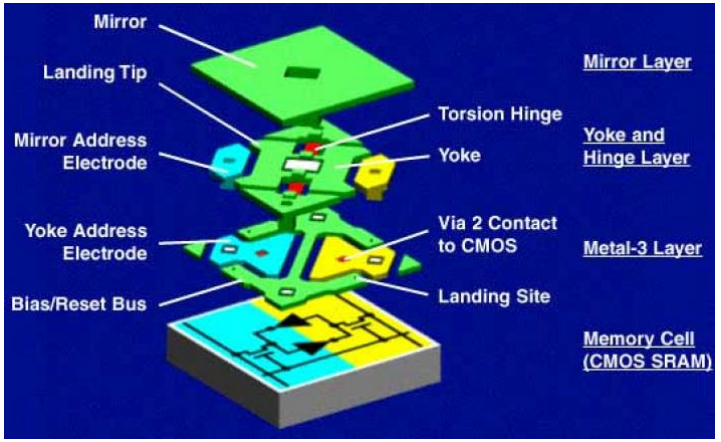


Completed Device

Mirror : Al alloy



device without mirror



post-processing on CMOS wafers
⇒ all process steps at T < 400°C

What is MEMS Technology?

1. Introduction to MEMS
2. **Common materials in MEMS**
3. Etching
4. Surface micromachining
5. Bulk micromachining
6. Molding

Silicon is the most widely used substrate for MEMS

- Single crystal silicon – SCS
  - Anisotropic crystal
  - Semiconductor, great heat conductor
- Polycrystalline silicon – polysilicon
  - Mostly isotropic material
  - Semiconductor
- Silicon dioxide – SiO_2
  - Excellent thermal and electrical insulator
  - Mask in etching of silicon substrates
  - Sacrificial layer
- Silicon nitride – Si_3N_4
  - Excellent electrical insulator
  - Ion-implantation masks and barrier to diffusion.
- Aluminum – Al
  - Metal – excellent thermal and electrical conductor

Electrical resistivity

Metal	ρ (10^{-6} Ω×cm)	Applications
Ag	1.58	Electrochemistry
Al	2.7	Elect interconnects Optical reflection
Au	2.4	High T elect interconnect Optical refl IR electrochemistry
Cr, Ti, TiW	12.9, 42, 75-200	Intermediate adhesion layer
Cu	1.7	Elect interconnects
ITO	300-3000	Transparent interconnects
Ir, Pt	5.1, 10.6	Electrochemistry Bio-potential sensors
W	5.5	High T elect interconnects

Thermal conductivity

Material	At 300K (W/m K)
Si (SCS)	156
Si_3N_4	1.9
SiO_2	1.4
W	178
Al	236
Au	300

Thermal Expansion

Material	At 300K (10^{-6}/°C)
Si (SCS)	2.616
Si_3N_4	2.8
SiO_2	0.4-0.55
W	4.5
Al	25

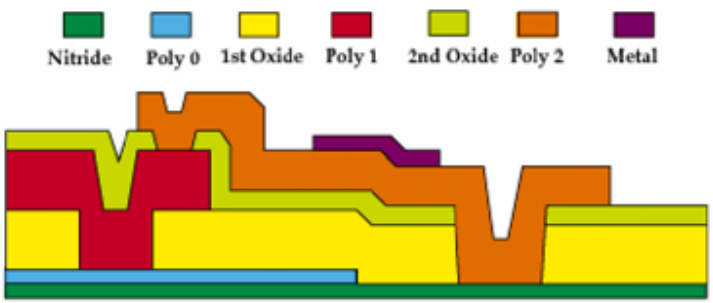
Yael Hanein

Why Silicon?

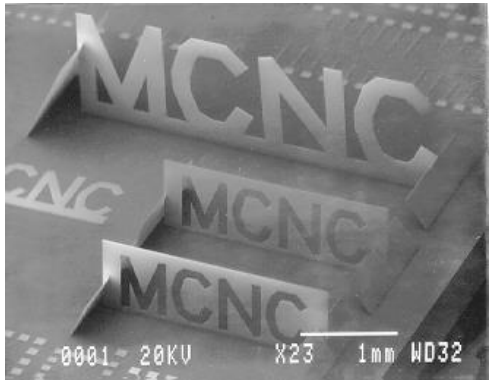
- Well understood and controllable electrical properties
- Availability of existing design tools
- Economical to produce single crystal substrates
- Desirable mechanical Properties:
  - High melting point. (1400 °C)
  - Small thermal expansion coefficient, 10 times smaller than Al
  - High Young's modulus (same as steel ~ 2 x 105MPa)
  - Light as aluminum (density ~ 2.3 g/cm3)
  - No mechanical hysteresis(Good candidate for sensors and actuators)
- Crystalline orientation is important in MEMS fabrication processes
- Integration with electronics on same substrate

Multi-User MEMS Process (MUMPs)

- Standardized building blocks for MEMS processing and MEMS components.
- MUMPs is a well-established, commercial program that provides customers with cost-effective access to MEMS prototyping and a smooth transition into volume manufacturing.
- MUMPs is part of MEMSCAP's complete manufacturing offer, ranging from prototyping to mass production.
- MUMPs was first offered by MCNC in 1992. Cronos was spun –off from MCNC in 1999 to provide MUMPs



PolyMUMPs Process



MUMPs (1993, MCNC)

Microelectronics Center of North Carolina

A gear train on a moving platform.

SUMMiT IV (1998)

Sandia National Laboratory)

Features:

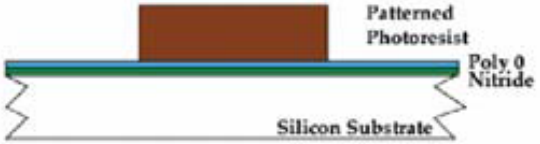
- Structural material: Polysilicon
- Sacrificial layer: Deposited oxide (PSG)
- Electrical isolation: silicon nitride
- 3 polysilicon layers

http://www.memscap.com/memsrus/crmumps.html

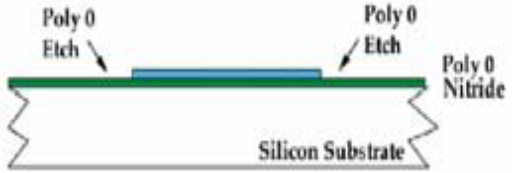
PolyMUMPs Process Flow

- N+ doping
- Silicon nitride (Nitride) deposition (600nm)
- 500 nm polysilicon (Poly 0) deposition
- Photoresist coating

- Photolithography using first level mask (POLY0)

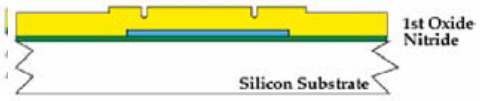


- RIE Poly0
- Photoresist stripping (in a solvent)

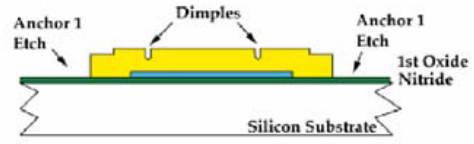


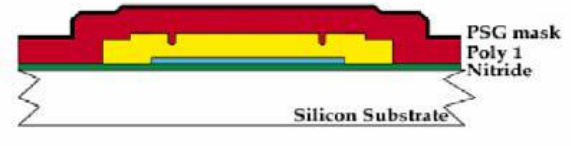
- 2.0 µm LPCVD PSG deposition (the first sacrificial layer)

- Second mask (DIMPLE) patterned
- The dimples, 750 nm deep, are etched (RIE) into the first oxide layer.



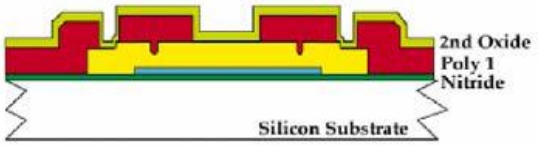
- Third mask (ANCHOR1) patterned



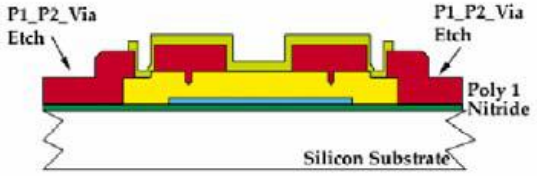


- A blanket 2.0 µm layer of un-doped polysilicon is deposited by LPCVD followed by the deposition of 200 nm PSG and a 1050° C/1 hour anneal. The anneal serves to both dope the polysilicon and reduce its residual stress.

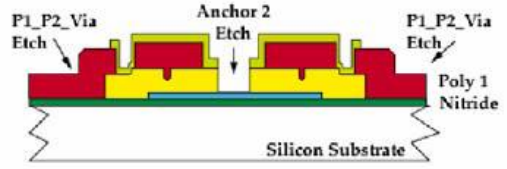
- The fourth mask (POLY1) is lithographically patterned. The PSG is first etched to create a hard mask and then Poly 1 is etched by RIE.
- After the etch is completed, the photoresist and PSG hard mask are removed.



- The Second Oxide layer, 0.75 µm of PSG, is deposited on the wafer. This layer is patterned twice to allow contact to both Poly 1 and substrate layers.



- The fifth mask (POLY1_POLY2_VIA) is lithographically patterned.
- The unwanted Second Oxide is RIE etched, stopping on Poly 1, and the photoresist is stripped.

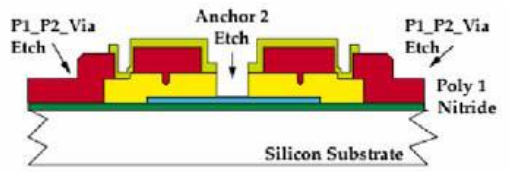


- The sixth mask (ANCHOR2) is lithographically patterned.
- Second and First Oxides are RIE etched, stopping on either Nitride or Poly 0, and photoresist is stripped.
- The ANCHOR2 level provides openings for Poly 2 to contact with Nitride or Poly 0.

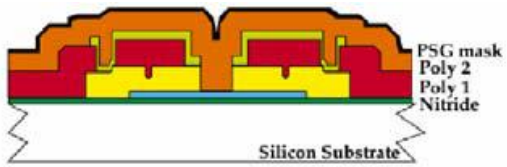
H.Xie & http://www.memscap.com/memsrus/svcsrules.html

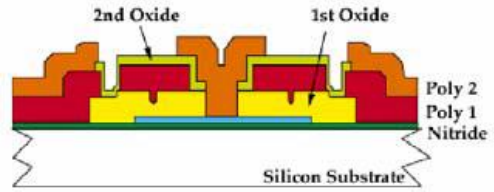
PolyMUMPs Process Flow (cont'd)

- The sixth mask (ANCHOR2) is lithographically patterned.
- Second and First Oxides are RIE etched, stopping on either Nitride or Poly 0, and photoresist is stripped.
- The ANCHOR2 level provides openings for Poly 2 to contact with Nitride or Poly 0.

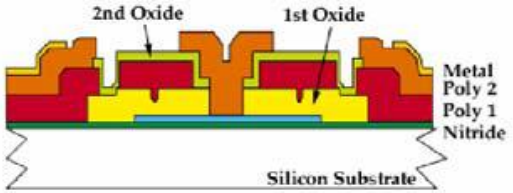


- A 1.5 μm un-doped polysilicon layer is deposited followed by a 200 nm PSG hardmask layer. The wafers are annealed at 1050°C for one hour to dope the polysilicon and reduce residual stress.



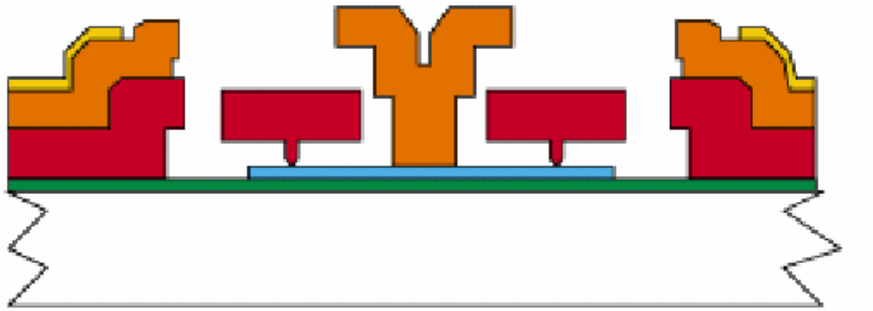


- The seventh mask (POLY2) is lithographically patterned.
- The PSG hard mask and Poly 2 layers are RIE etched and the photoresist and hard mask are removed.
- All mechanical structures have now been fabricated. The remaining steps are to deposit the metal layer and remove the sacrificial oxides



- The eighth mask (METAL) is patterned. The metal (gold with a thin adhesion layer) is deposited by lift-off patterning.
- The photoresist and unwanted metal (atop the hotoresist) are then removed in a solvent bath.
- The process is now complete and the wafers can be coated with a protective layer of photoresist and diced. The chips are sorted and shipped.

- The structures are released by immersing the chips in a 49% HF solution.
- The Poly 1 ``rotor" can be seen around the fixed Poly 2 hub.
- The stacks of Poly 1, Poly 2 and Metal on the sides represent the stators used to drive the motor electrostatically.



http://www.memscap.com/memsrus/svcsrules.html

What is MEMS Technology?

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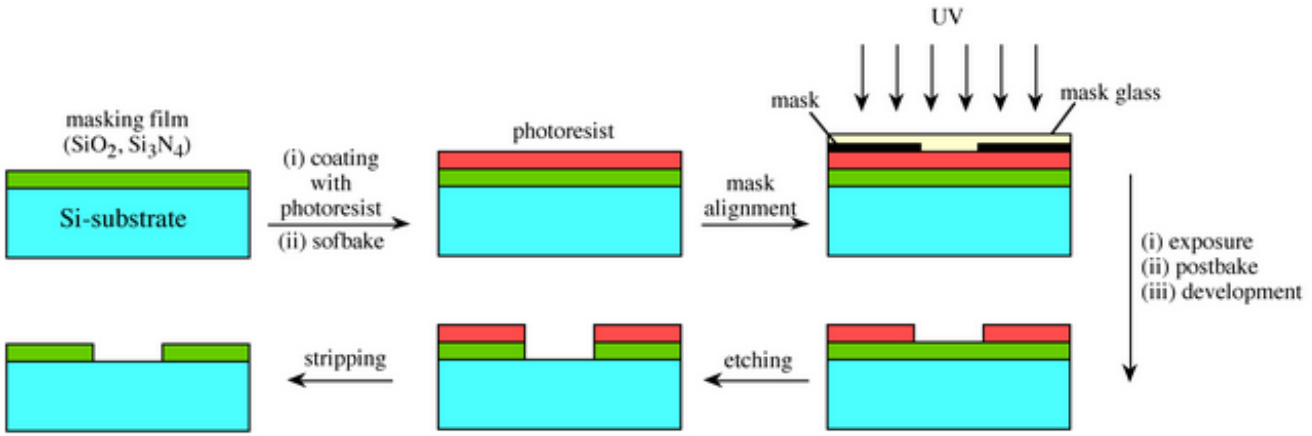
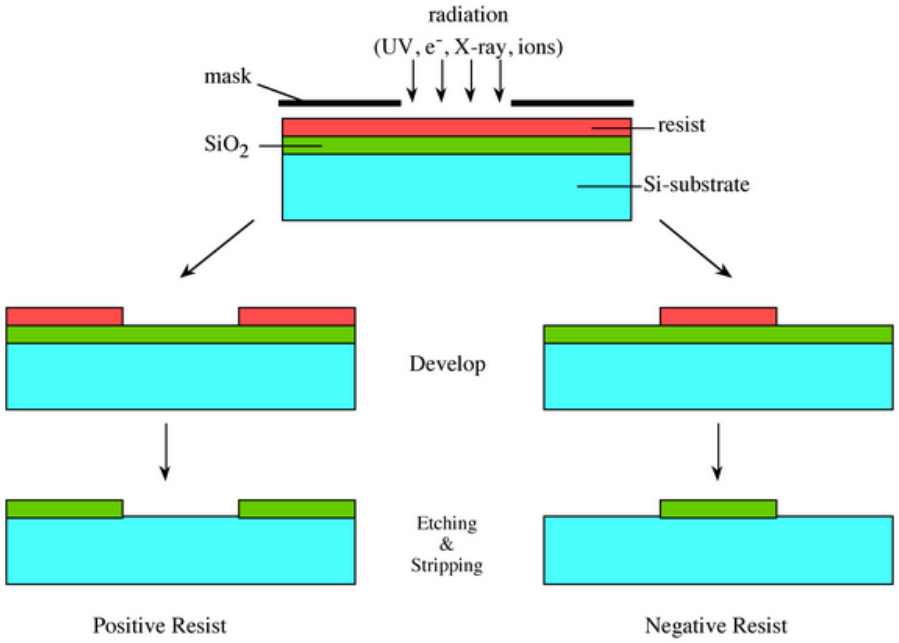
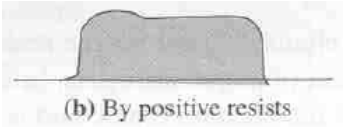
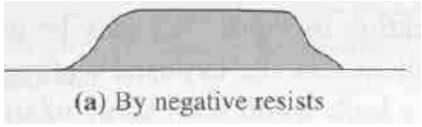
5. Bulk micromachining
6. Molding

General Procedure for Photolithography



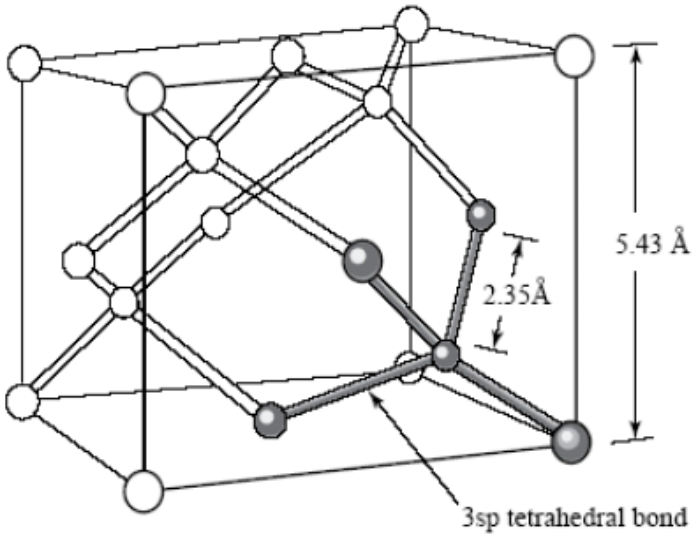


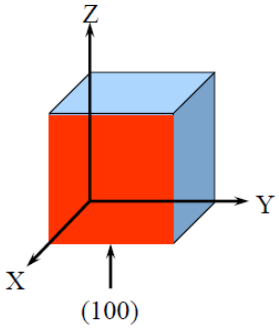


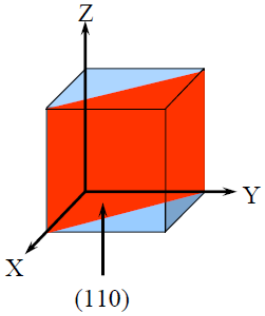


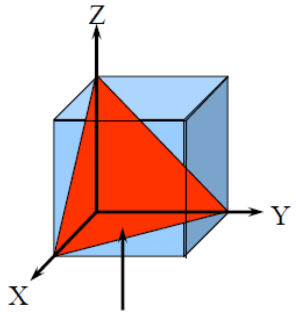
Andrew Barron (Rice University)

Orientation of Silicon Wafer

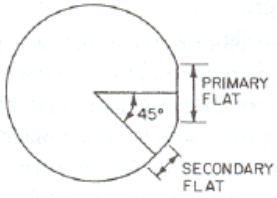




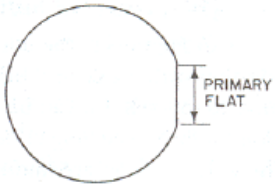




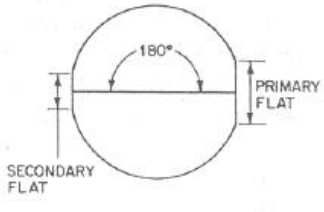
Flats are not found in large dia., >6"



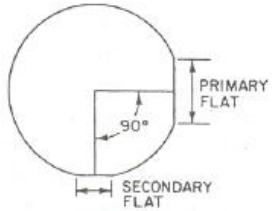
(111) n-type



(111) p- type



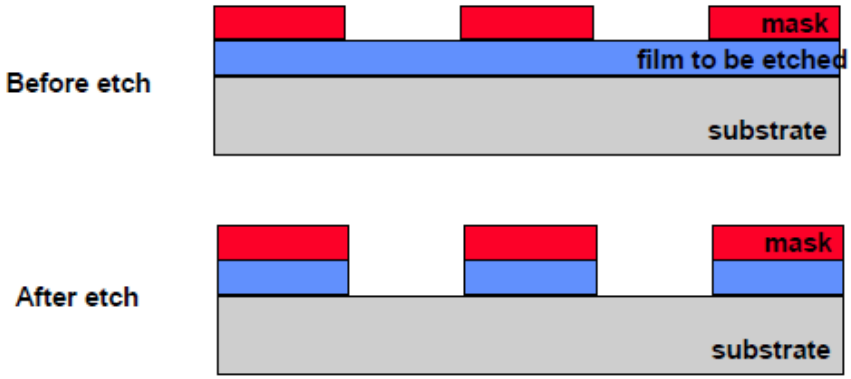
(100) n-type



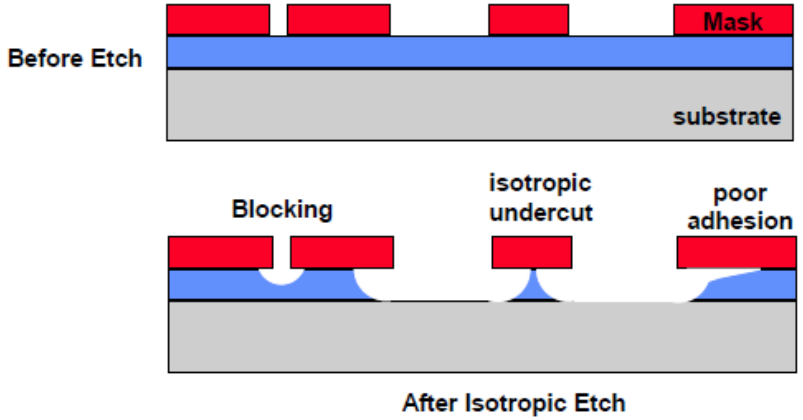
(100) p-type

Location of primary and secondary flats

Ideal Etching Process

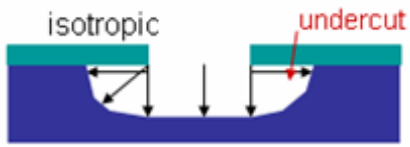


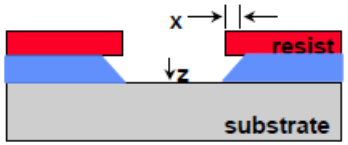
Wet Etching Problems



After Isotropic Etch

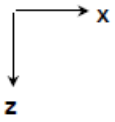
Directionality of Etching

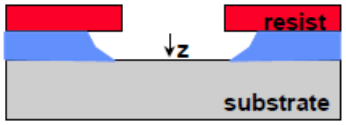




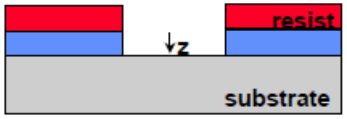
Anisotropic Etch (x < z) 0 < A < 1

Degree of Anisotropy
A = (z-x)/z





Isotropic Etch (x = z) A = 0

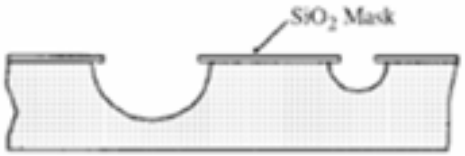


Vertical Etch (x = 0) A = 1
(Perfectly anisotropic)

Isotropic Wet Etching
Poly- Etch & Buffered-Oxide-Etch

- Etch rate: 4-20 μm/min
- Etch masks: Si_3N_4 and SiO_2
- SiO_2 fairly attacked (30- 70 nm/sec)
- Agitation speeds up process
- Slows down in light doping (10^{17} cm^{-3} n/p)

ISOTROPIC WET ETCHING: AGITATION



ISOTROPIC WET ETCHING: NO AGITATION

(a)

(1) Poly-etch HNA: HF/HNO3/HC2H3O2

$$HNO_3\ (aq) + Si(s) + 6HF\ (aq) \rightarrow H_2SiF_6\ (aq) + HNO_2\ (aq) + H_2O\ (l) + H_2\ (g)$$

The etching process actually occurs in several steps.

First step, nitric acid oxidizes the silicon

$$HNO_3\ (aq) + H_2O\ (l) + Si\ (s) \rightarrow SiO_2\ (s) + HNO_2\ (aq) + H_2\ (g)$$

In the second step, the newly formed silicon dioxide is etched by the hydrofluoric acid.

$$SiO_2\ (s) + 6HF\ (aq) \rightarrow H_2SiF_6\ (aq) + 2\ H_2O\ (l)$$

(2) BOE (Buffered Oxide Etch): HF/NH4F/H2O

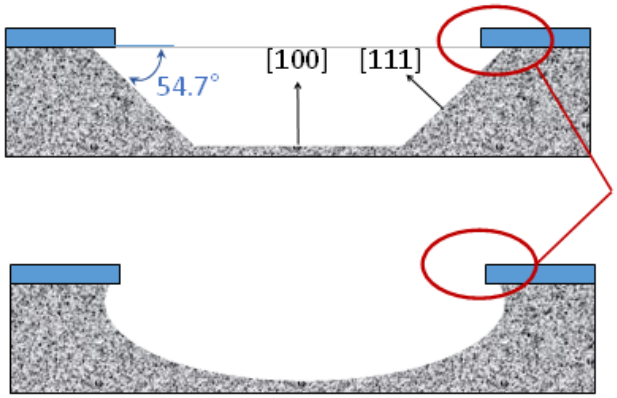
Used in isotropic etching of silicon dioxide and glass

Jack W Judy, "Microelectromechanicalsystem (MEMS): fabrication, design and application," Smart Materials And Structures, IEEE Review Paper,November 2001.

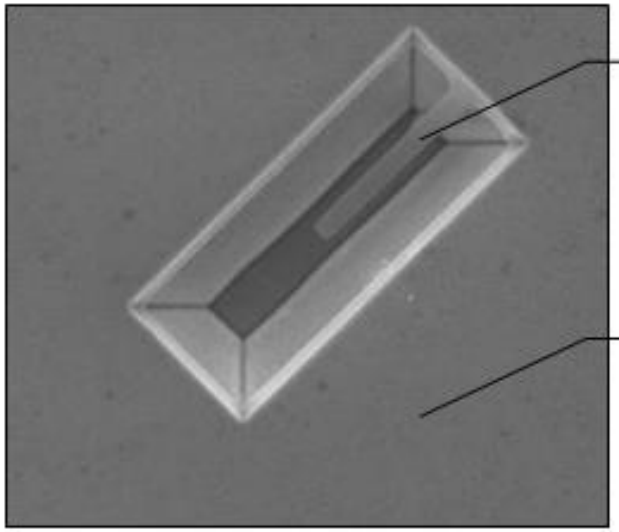
Selectivity and Undercutting

Selectivity

- Etch rate of one material compared to another.
- Etch rate of one direction compared to another.

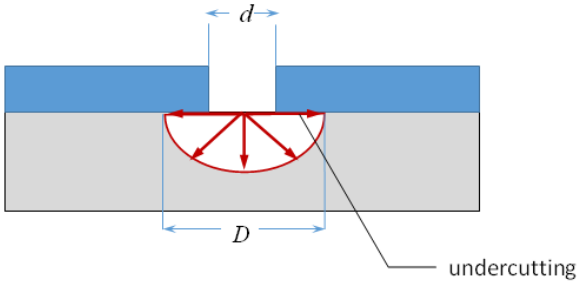


Undercutting



SEM image of a SiO2 cantilever formed by undercutting

(S. Mohana Sundaram and A. Ghosh,)

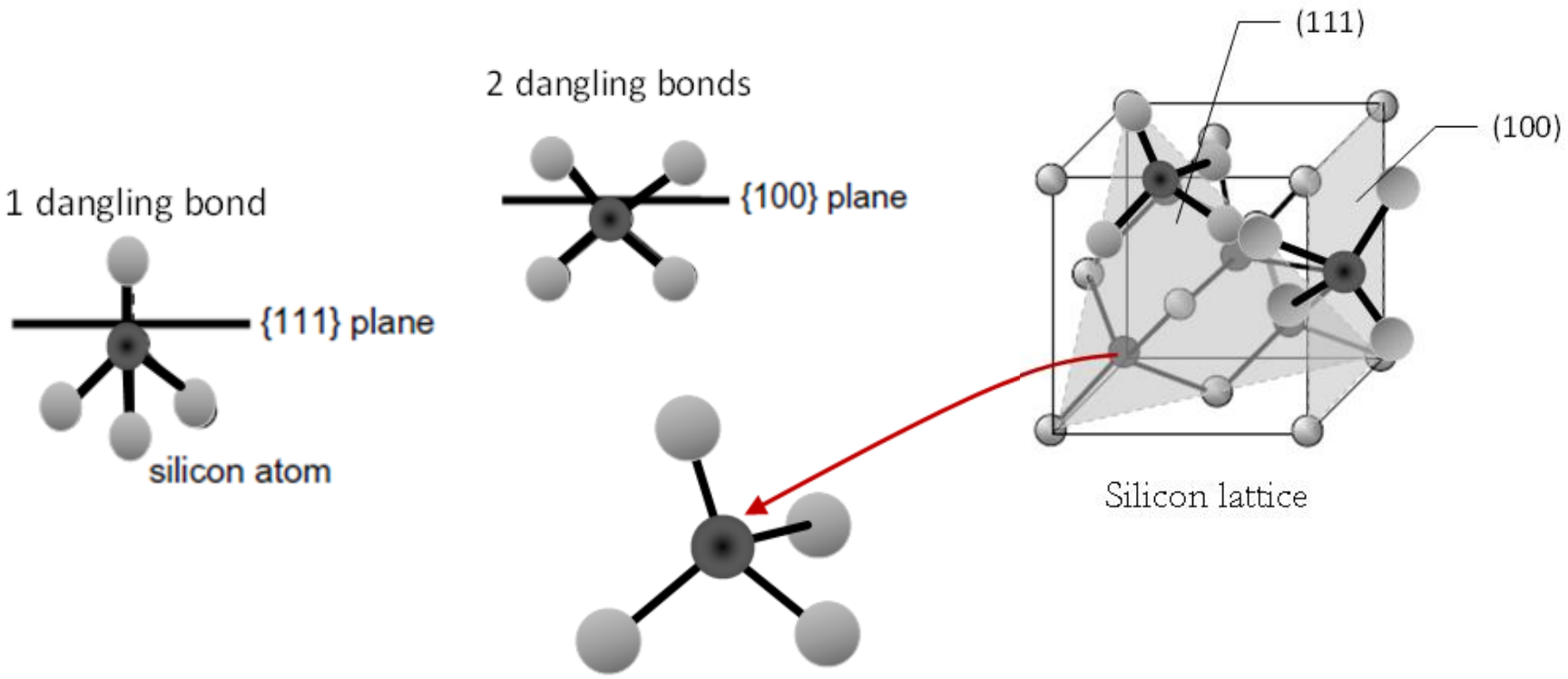


Estimate of etch depth

depth ≈ $(D-d)/2$

Resulting undercutting can be used to create suspended structures!

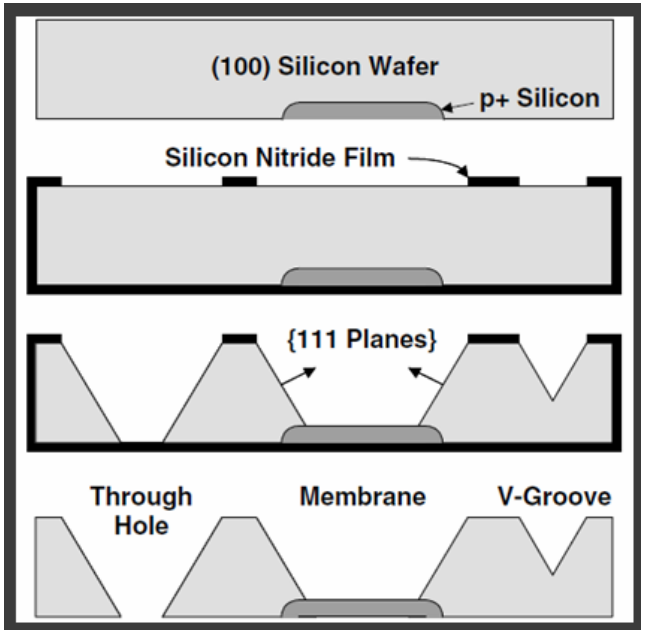
The Lower Reaction Rate For The (111) Planes



The lower reaction rate for the (111) planes is caused by the larger activation energy required to break bonds behind the etch plane. This is due to the larger bond density of silicon atoms behind the (111) plane.

(Siedel *et al.*)

Anisotropic Wet Etching



Etchant	Temperature(°C)	Etch rate(μm/hr)		
		Si (100)	Si(110)	Si(111)
KOH	75	25-42	39-66	0.5
EDP	110	51	57	1.25
NH_4OH	75	24	8	1

- Masks :
  - SiO_2 : for short period
  - Si_xN_y : Excellent
  - Heavily doped P^{++} silicon ; etch stop

TMAH: (100) 0.5-1.5 μm/min

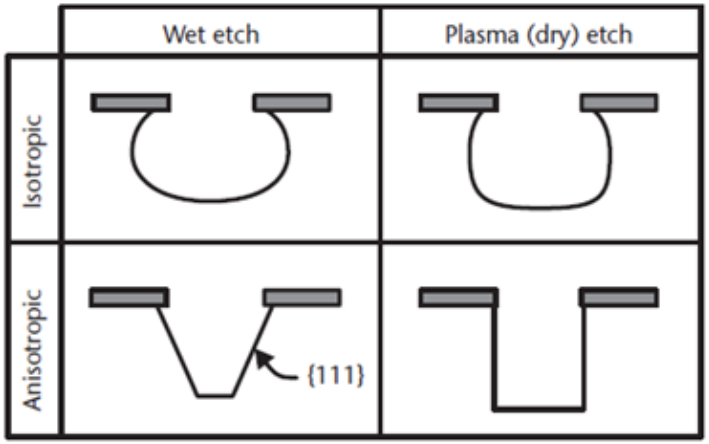
KOH etching smoother than EDP and NH4OH

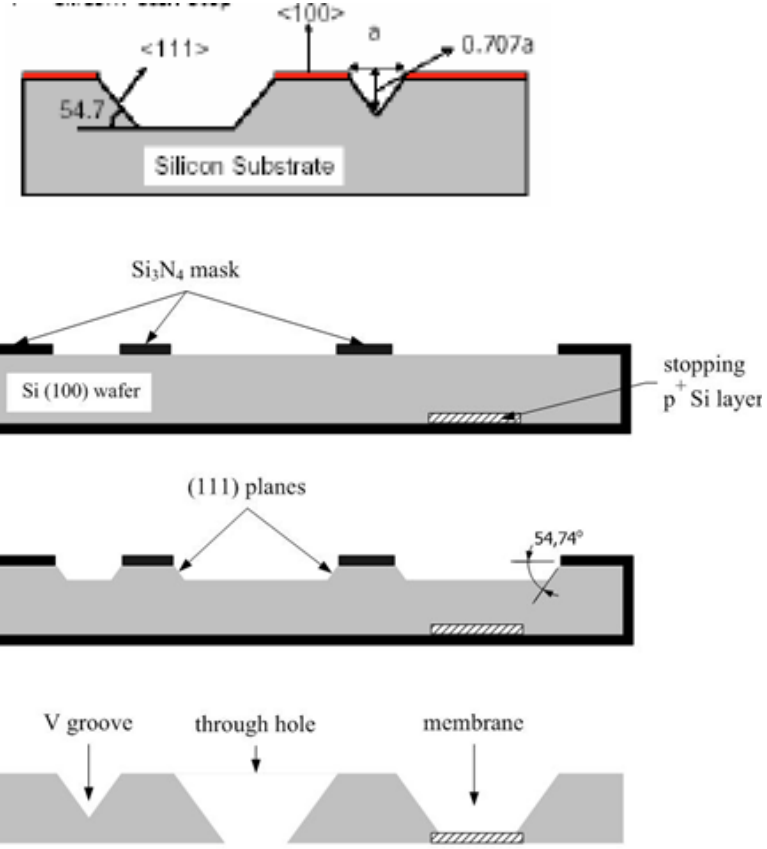
Van Zeghbroek : « Principles of Semiconductor Devices », 2005

T. A. Kovacs, Nadiml. Maluf, Gregory And Kurt E. Petersen, "Bulk Micromachining of Silicon,"IEEEReview Paper, August 1998.

Anisotropic Etching

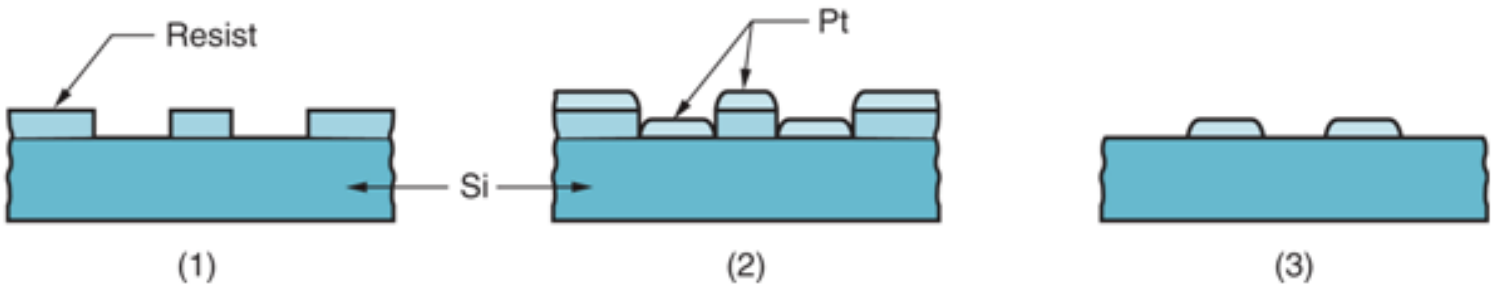
- The etch proceeds in the <100> direction, which is the vertical direction in (100) oriented substrate.
- The V-shaped trench is a result of the self-limits on four equivalent but intersecting {111} planes.



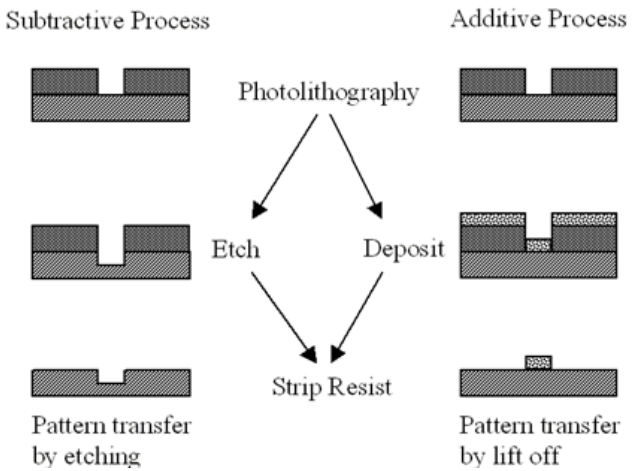


Lift-off Technique in Microfabrication

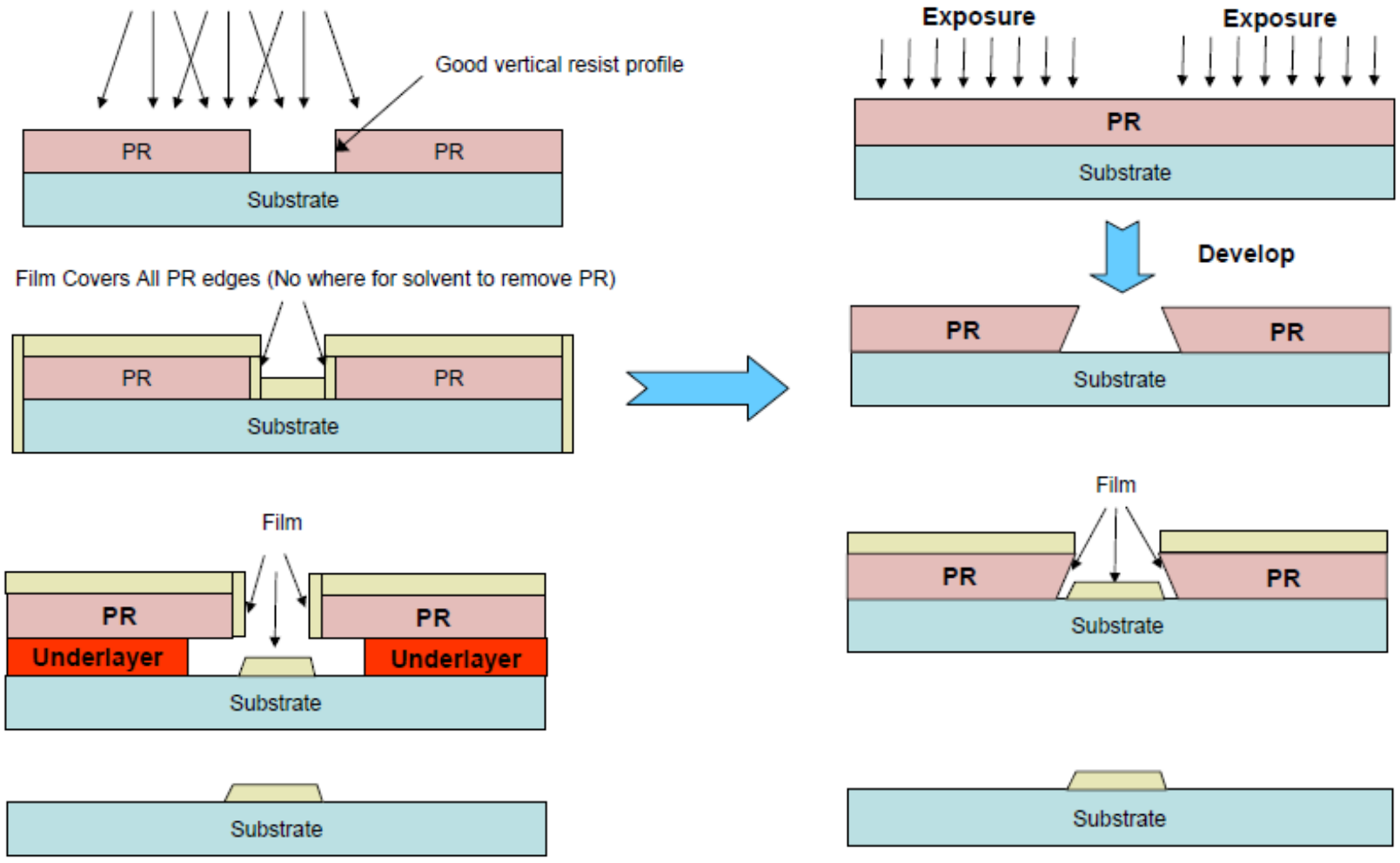
- ✓ To pattern metals such as platinum on a substrate for use in certain chemical sensors
- ✓ Process: (1) resist is applied to substrate and structured by lithography, (2) platinum is deposited, (3) resist is removed, lifting Pt but leaving desired Pt microstructure



M.P. Groove : Fundamentals of Modern Manufacturing, 4th Edition, John Wiley & Sons, Inc. 2010.



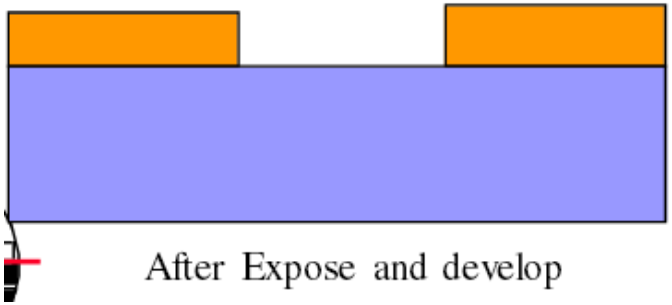
Lift-off Techniques



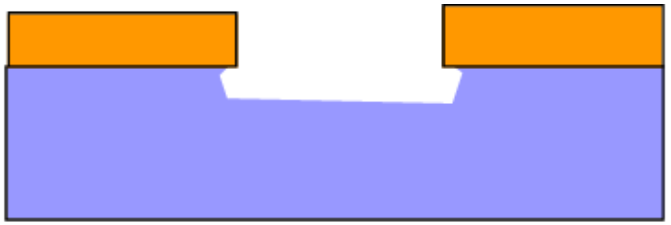
Lift-off Techniques. Single Layer Resist & Substrate Etch (Lynn Fuller)

Starting glass wafer 500um thick

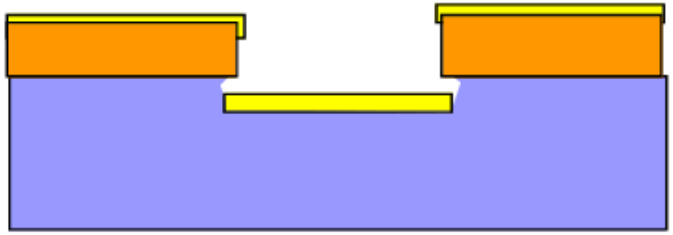
OIR-620-10 Positive Photoresist



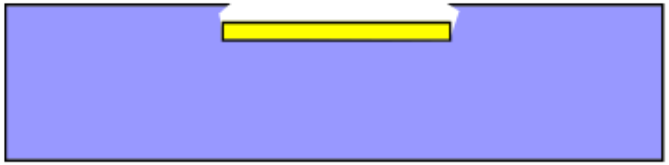
After Expose and develop



BOE etch to create undercut



Deposit Cr and Au



Lift-Off in Acetone and ultrasonic

Dry Etching

Advantages

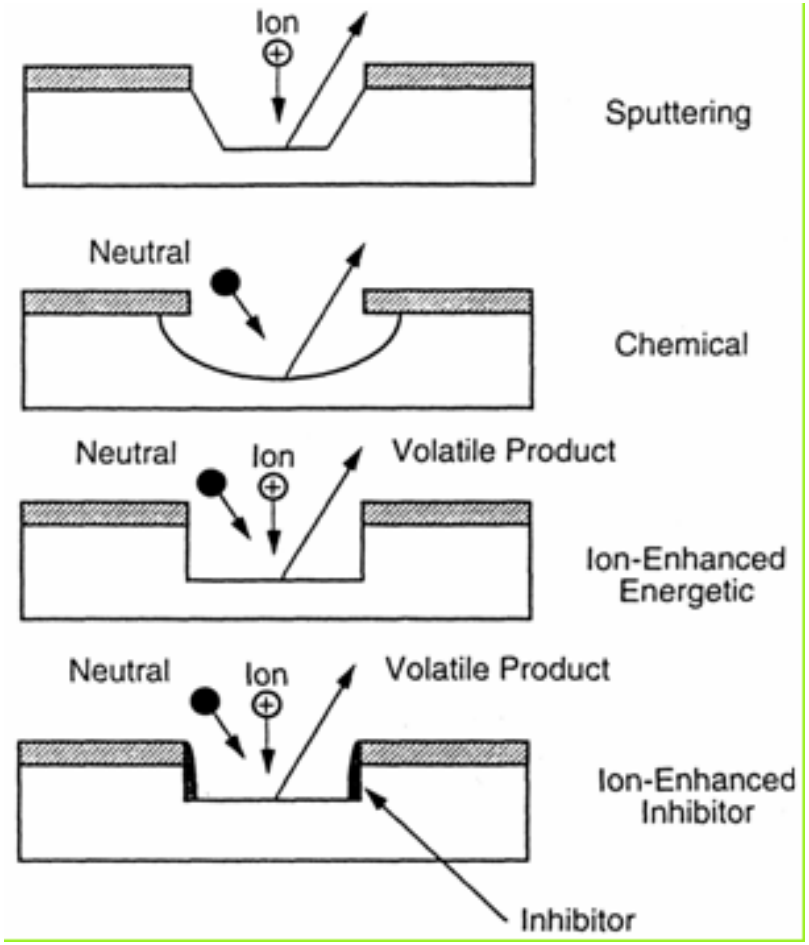
- Eliminates handling of dangerous acids and solvents
- Use small amount of chemicals
- Directional etching, less dependent on the crystal orientation of Si
- Good transfer of patterns
- High resolution and cleaniness
- Less undercutting
- No unintentional prolongation of etching
- Better process control
- Ease of automation

Disadvantages

- Some gases are toxic and corrosive
- Re-deposition of non-volatile compounds
- Needs for specialized equipment

Anisotropic etching

- **Sputter etching: belongs to plasma etching category. Similar principle to sputtering but the substrate is now subjected to ion bombardment.**
- **Chemical (vapor phase etching): the material is dissolved at the surface in a chemical reaction with the gas molecules.**
- **RIE:under RF, the gas molecules break into ions; and the ions accelerate and react the the surface of the material to be etched**
- **DRIE: the balance of chemical and physical etching to give vertical shapes.**



Types of Dry Etching

- ✓ **Non-plasma based:** ***spontaneous reaction of appropriate reactive gas mixture.***

  (i) ***Typically fluorine-containing gases, such as xeron difluoride XeF_2 and interhalogen BrF_3 and ClF_3; (ii) High selectivity to masking layers; (iii) no plasma processing equipment is required; (iv) controlled by temperatures and pressure of reactants.***

- ✓ **Plasma based:** ***RF power to drive chemical reaction.***

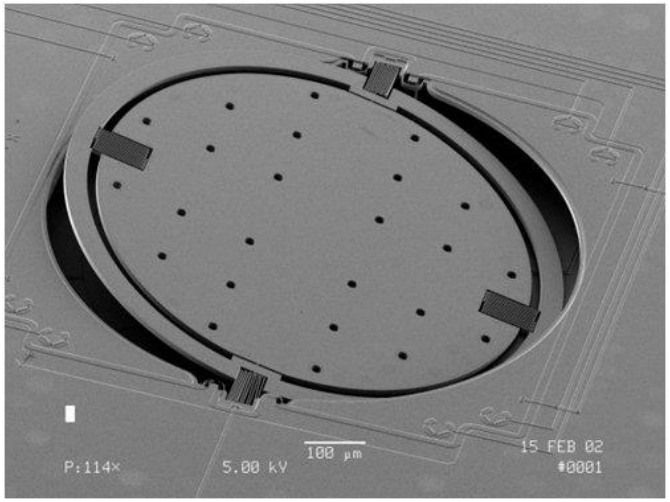
Xenon Difluoride (XeF_2) Etching

- Isotropic etching of Si
- High selectivity for Al, SiO_2, Si_3N_4, PR, PSG
- $2XeF_2 + Si \rightarrow 2Xe + SiF_4$
- Typical etch rates of 1 to 3 μm/min
- Heat is generated during exothermic reaction
- XeF_2 reacts with water (or vapor) to form HF

Interhalogen (BrF_3 & ClF_3) Etching

- Nearly isotropic profile
- Gases react with Si to form SiF_4
- Surface roughness: ~40 to 150 nm
- Masks: SiO_2, Si_3N_4, PR, Al, Cu, Au, and Ni

(From Tianghong Cui)

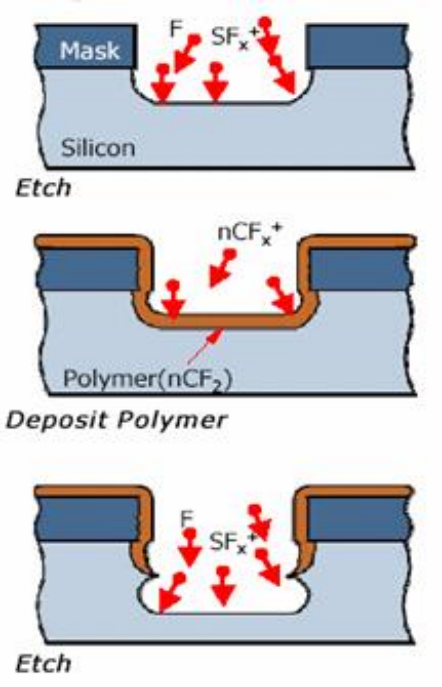


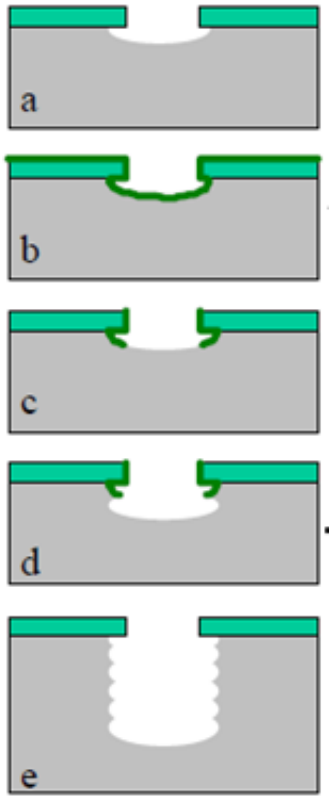
XeF_2 etching (stiction free release)

Alex Mintz

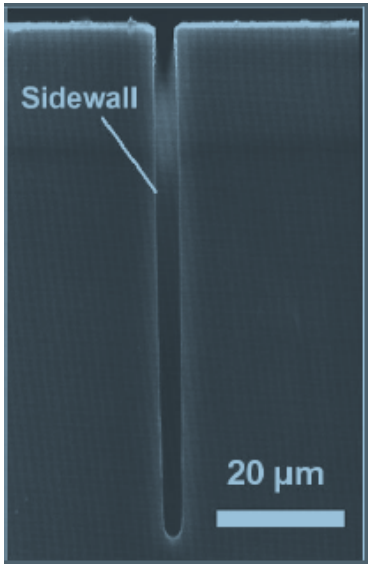
Deep reactive ion etching (DRIE, Bosch, 1994)

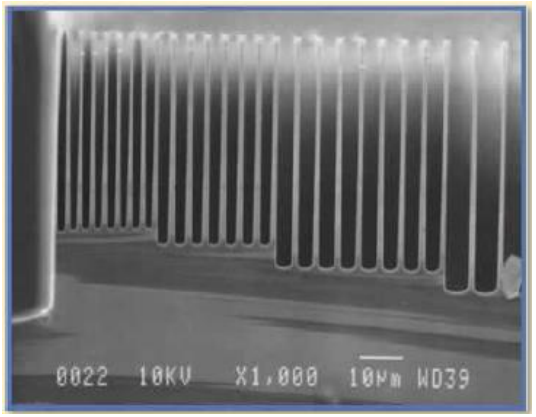
- Etch depths of hundreds of microns. Etching with SF4 (5-15s) and depositing with C4F8 (5-15s)
- Two different gas compositions are alternated in the reactor.
- The first gas creates a polymer on the surface of the substrate; and the second gas etches the substrate.
- The polymer is immediately sputtered away, but only on the horizontal surfaces, not the sidewalls.
- The polymer dissolves slowly in the chemical part of the etching and is built up on the sidewalls.





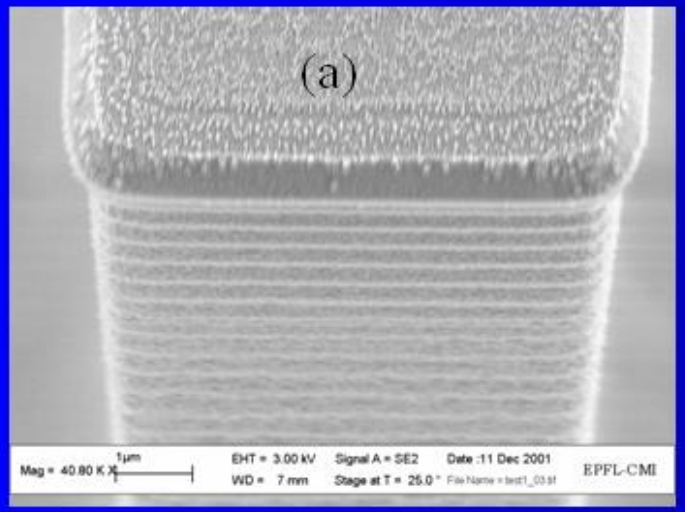
Profile of a DRIE trench using the Bosch process. Etching aspect ratio (ratio of height to width) of 50 to 1 can be achieved.

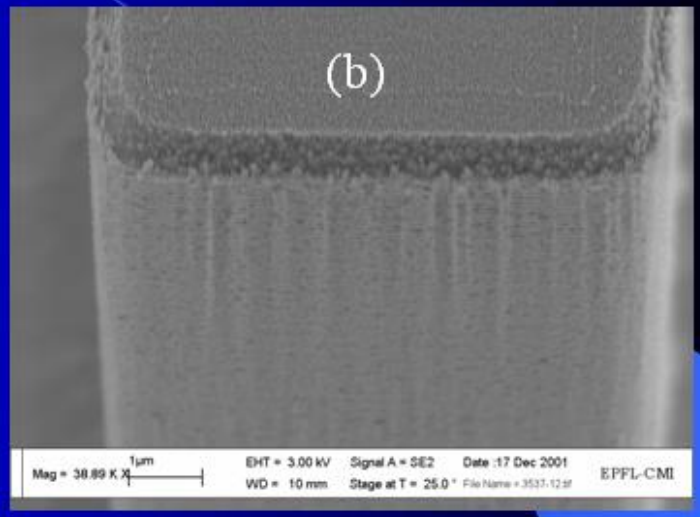




Trenches etched with DRIE [SEM images courtesy of Khalil Najafi, University of Michigan]]

Bosch process: sidewall roughness





Sidewall roughness at the top of a deep anisotropic etching of Si (Bosch process on A601E) as a function of pulse duration:
(a) SF6/C4F8 = 7s/2s (b) SF6/C4F8 = 3s/1s.

What is MEMS Technology?

1. Introduction to MEMS
2. Common materials in MEMS
3. Etching
4. **Surface micromachining**
5. Bulk micromachining
6. Molding

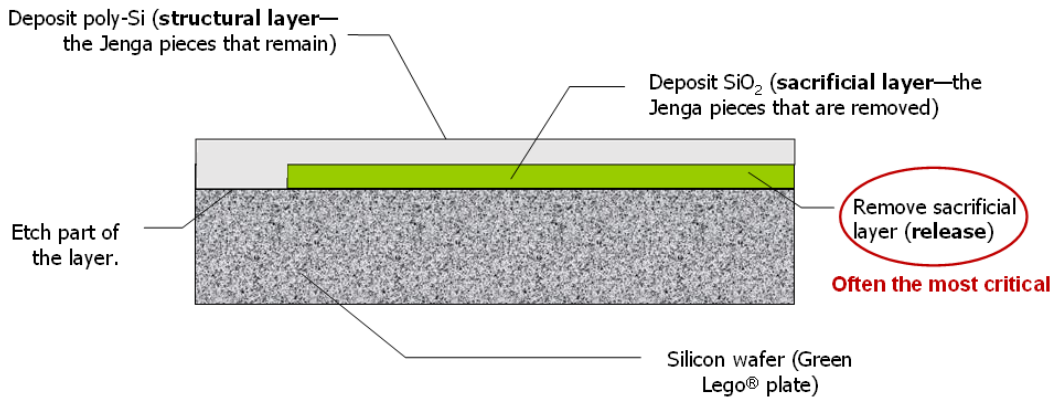
Surface Micromachining

The Si wafer functions like the big green flat plate.

+

Some Jenga pieces are removed. The ones that remain form the MEMS structure.

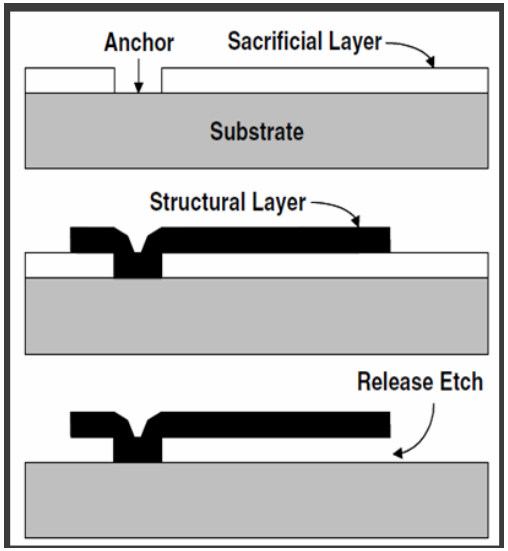
= Surface micromachining

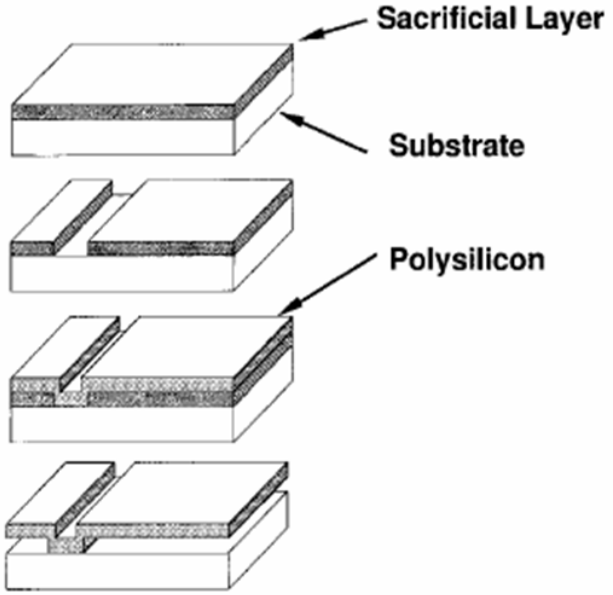


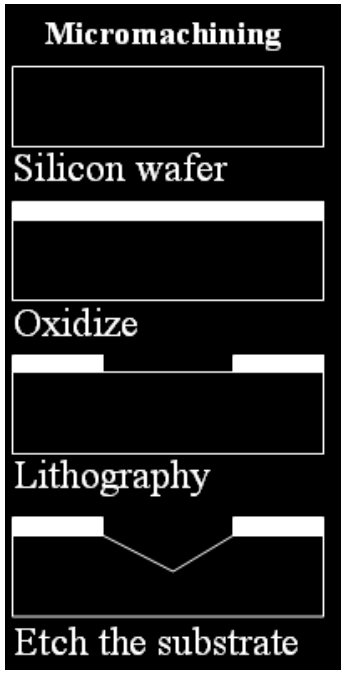
N. Maluf.

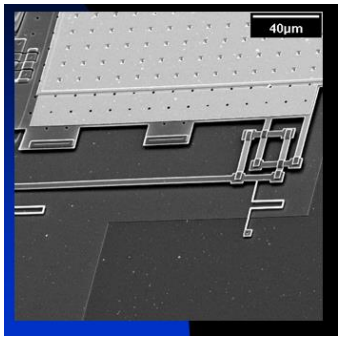
Polysilicon and Oxide for MEMS

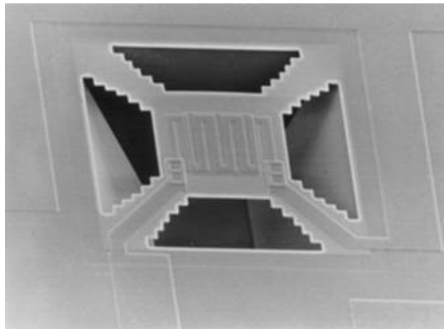
(A combination of sacrificial and structural layers)

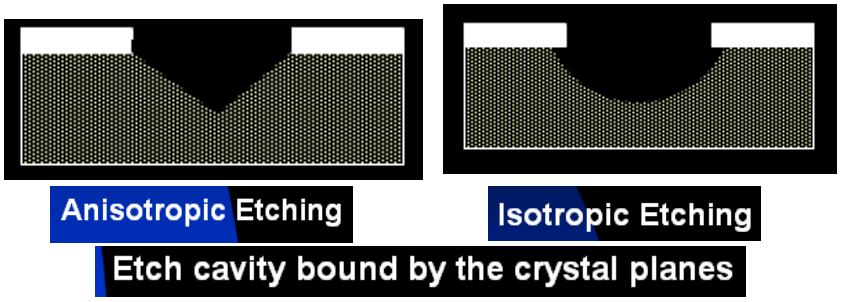






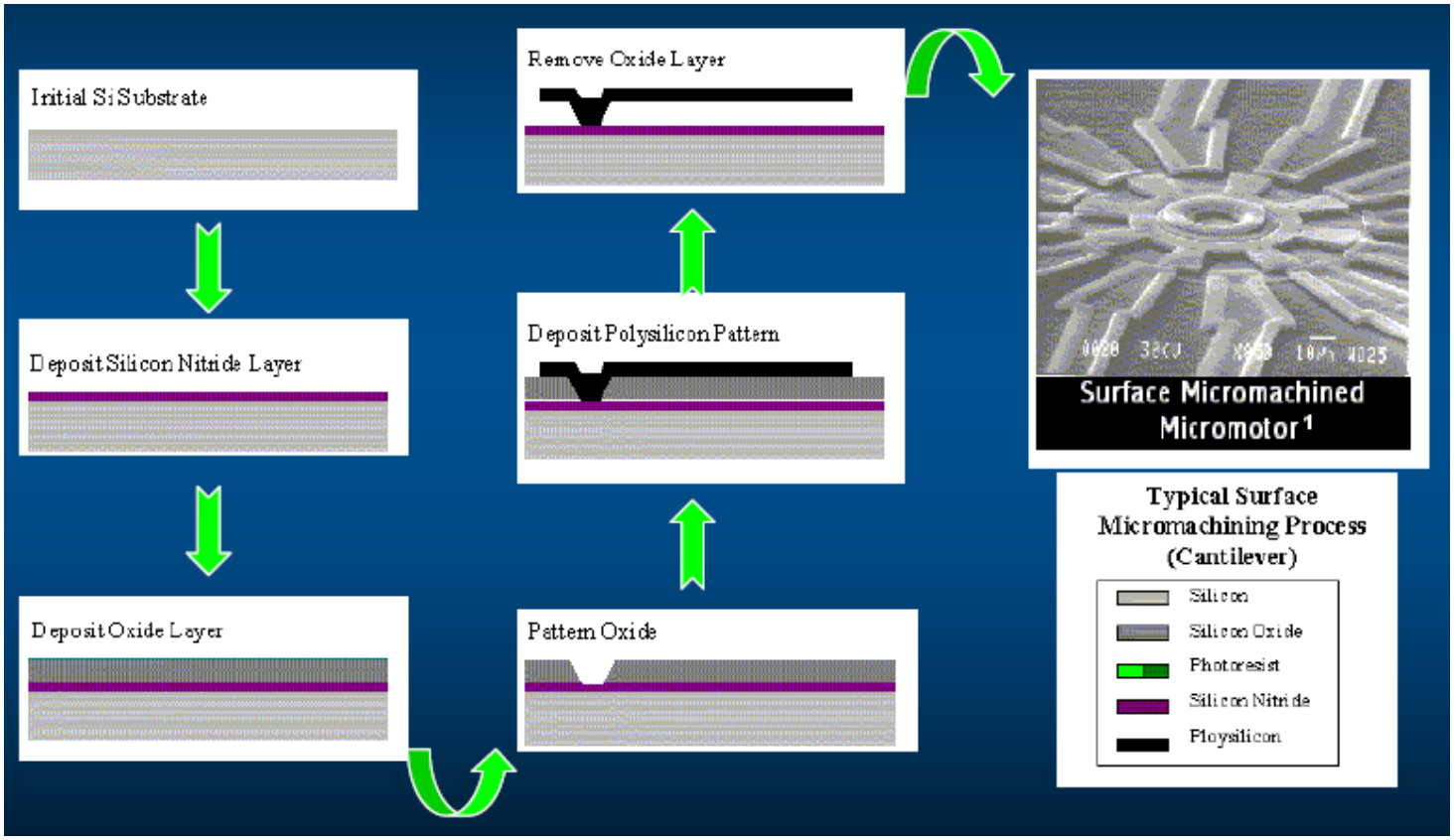






Robert W. Johnstone, SPIE 2002

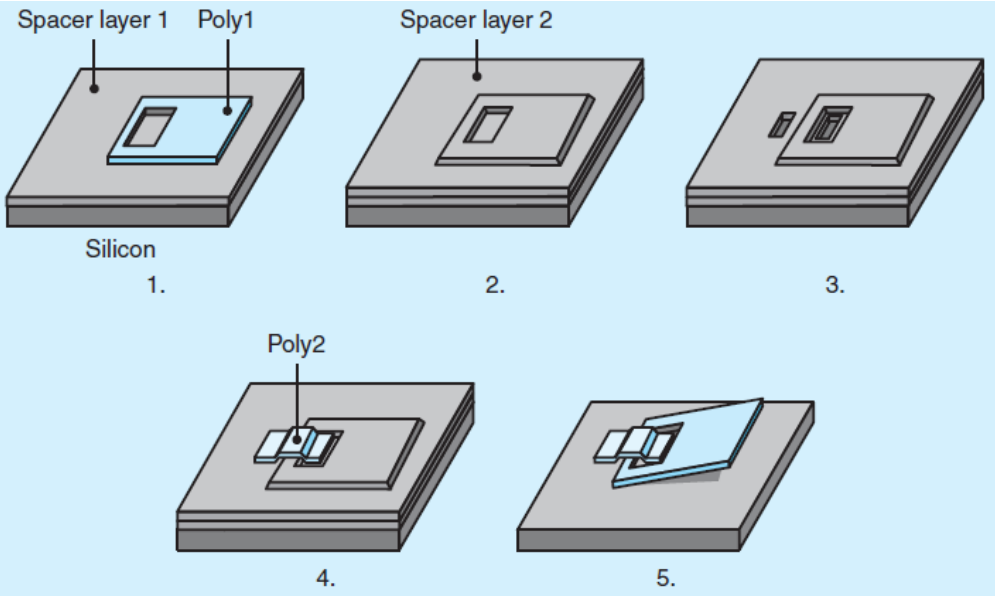
Surface Micromachining

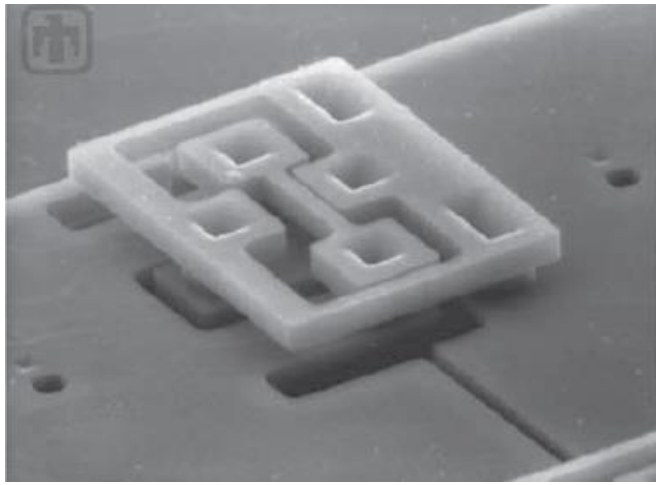


Y.C. Chen (TFIT)

Fabrication of a Hinge

1. A 2 μm layer of phosphorsilicate glass PSG spacer is deposited onto the substrate.
2. A 2 μm layer of polysilicon (poly 1 in step1) is deposited on PSG, patterned and dry etched to form the desired strcuture, including the hinge pins.
3. A second layer of sacrificial/space PSG (0.5 μm) is deposited (step 2)
4. The connection locations are selectively etched through both PSG layers (step 3).
5. A seond polysilicon (poly 2 in step 4) is deposited, patterned, and etched to form a staple for the hinge.
6. The sacrificial layers of PSG are then removed by wet etching. And the hinge can rotate



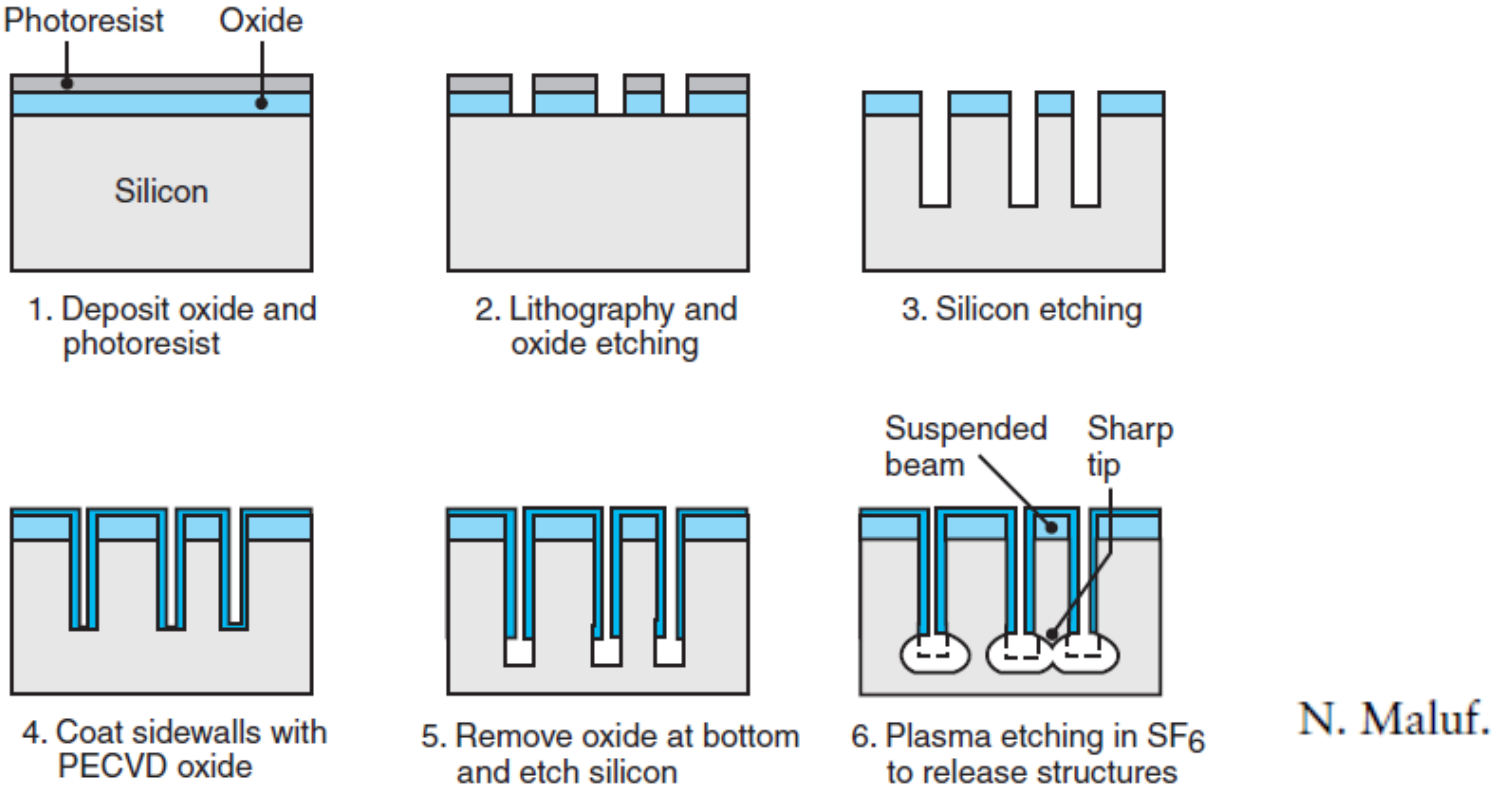


Detail of the micromirror hinge
(Sandia National Laboratories)

Fabrication of Microelectromechanical Devices and Systems by Kalpakjian

SCREAM

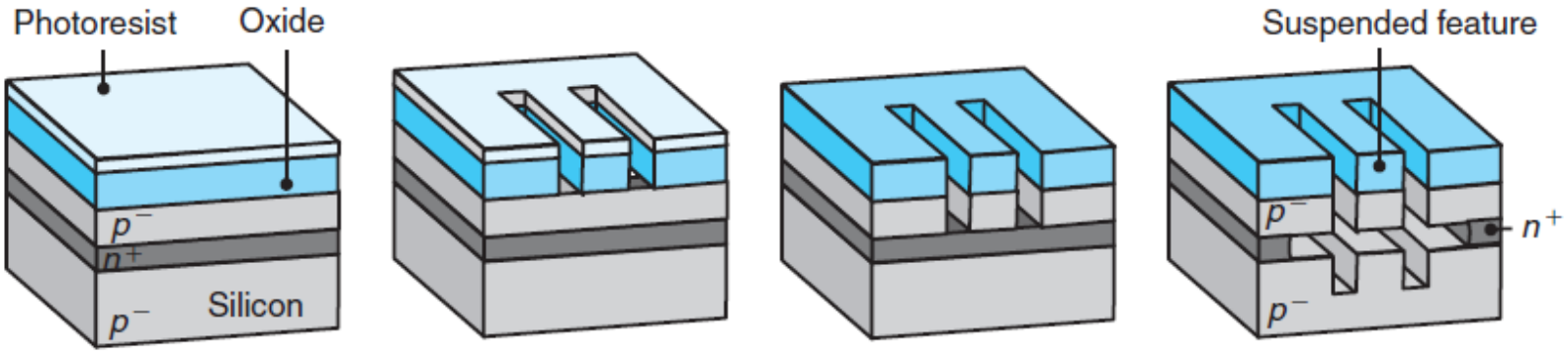
- **SCREAM: Single-Crystal silicon Reactive Etching And Metallization).**
- **Producing 10-50 μm deep, which is protected by a a layer of silicon oxide.**
- **An anisotropic etching removes the oxide only at the bottom of the trench, and the trench is extended through dry etching.**
- **An isotropic etching step (using sulfur hexafluoride) laterally etches the exposed sidewalls at the bottom of the trench. The undercut is used to release the structures.**



N. Maluf.

SIMPLE

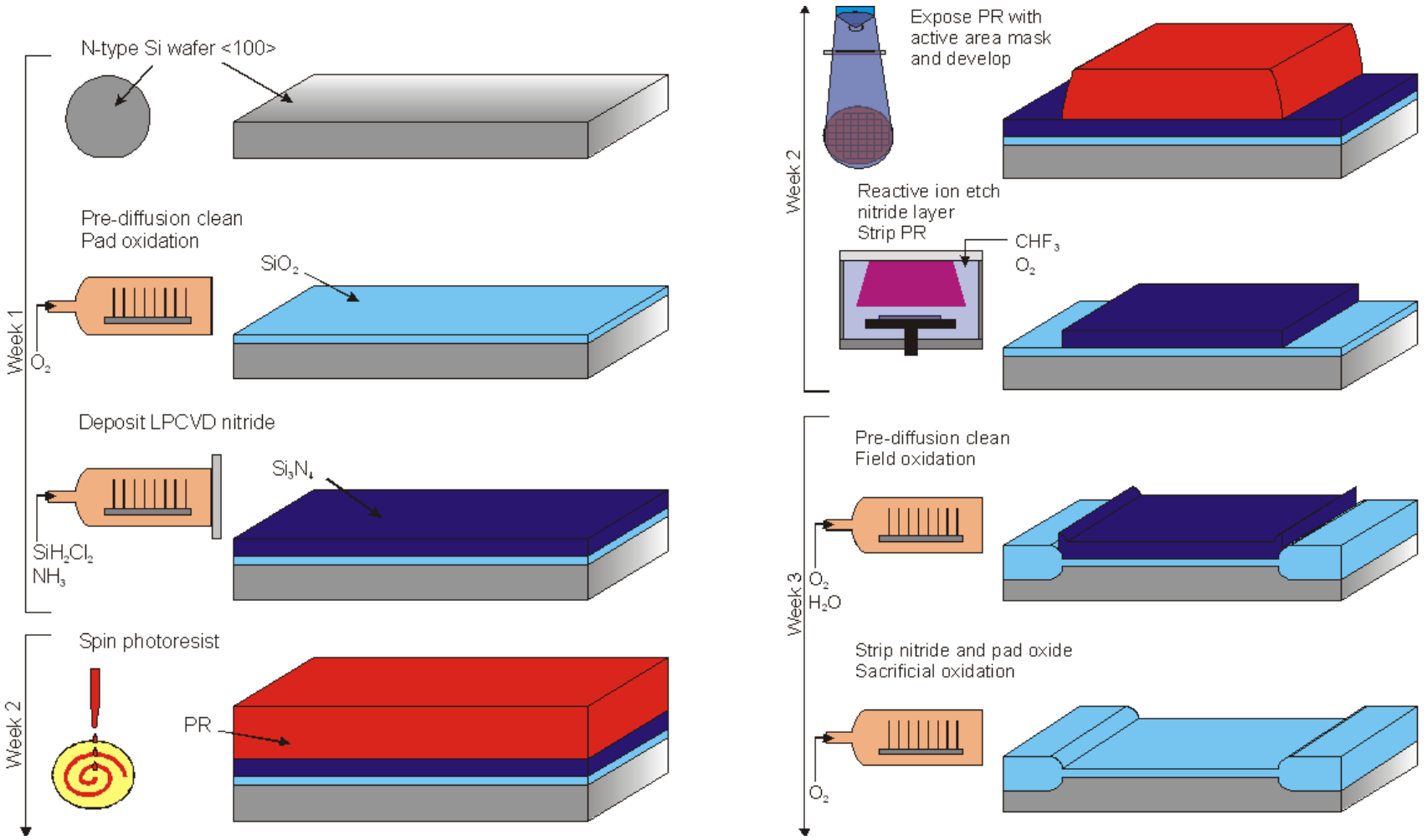
- SIMPLE: SIlicon Micromaching by single step PLasma Etching).
- One plasma-etching device.
- Chlorine gas-based plasma etching is used to etch p-doped or lightly doped silicon anisotropically, but heavily n-doped silicon isotropically.
- Thick oxide mask is required since chlorine –based plasma attacks the mask slowly.
- The isotropic etch rate is low, 50 nm/min.



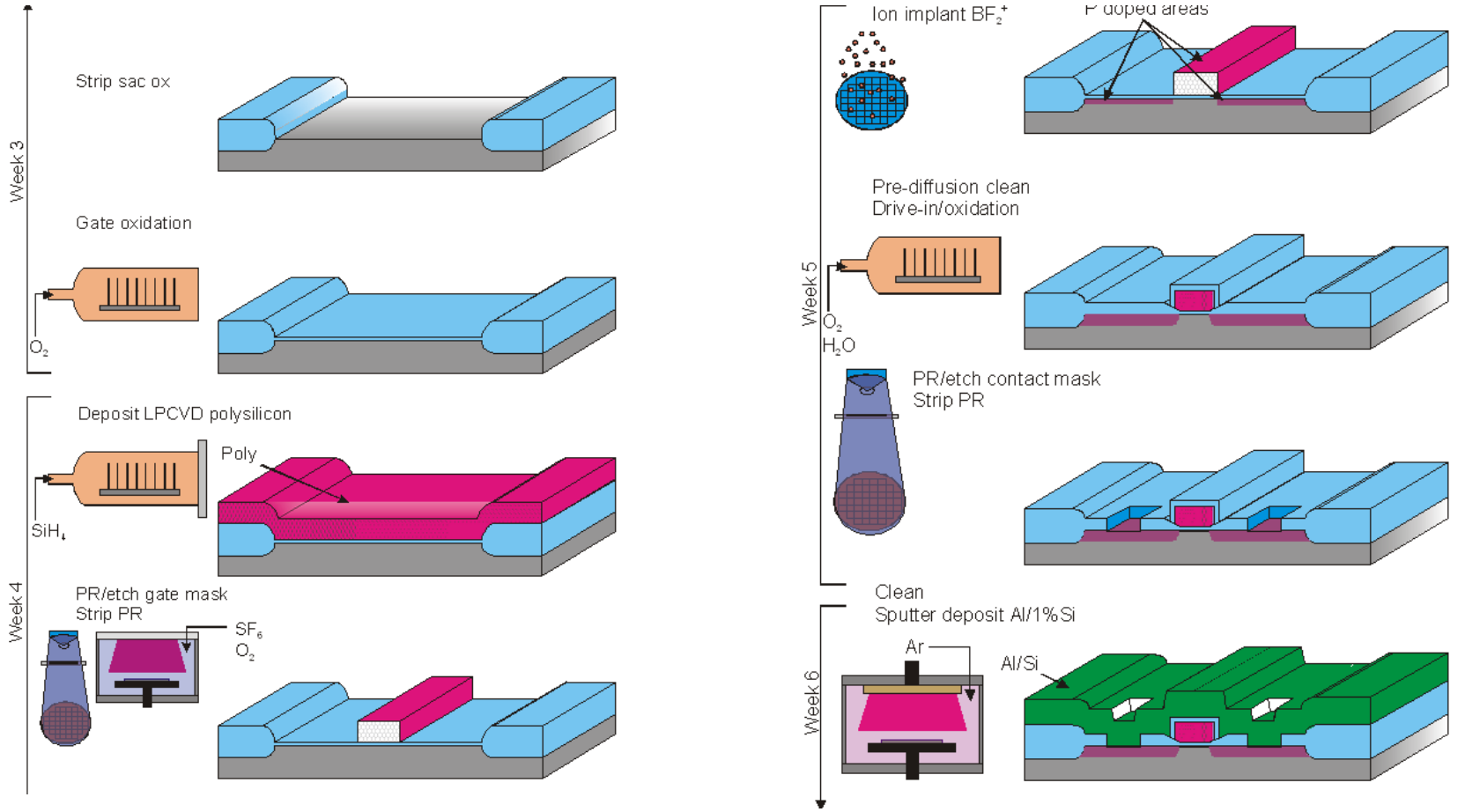
1. Deposit oxide and photoresist on layered substrate
2. Lithography and oxide etching
3. Plasma etching of p^- doped silicon
4. Isotropic etching of n^+ doped silicon

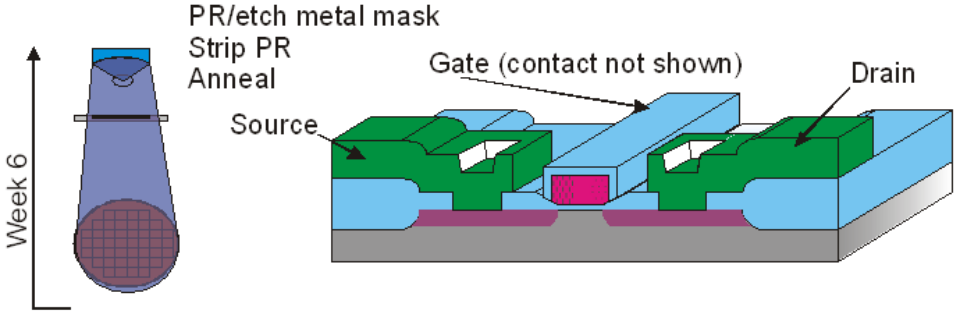
N. Maluf.

PMOS Fabrication Process (UCB)



PMOS Fabrication Process (cont'd)

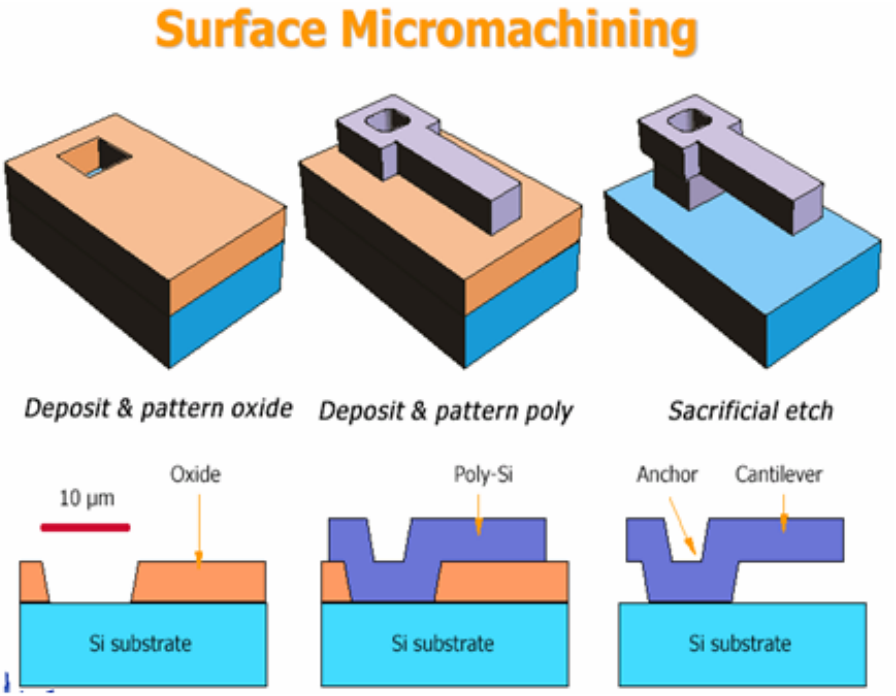




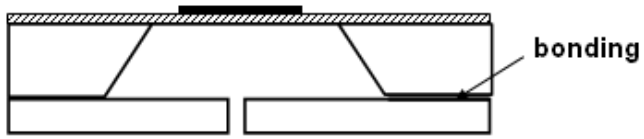
What is MEMS Technology?

1. Introduction to MEMS
2. Common materials in MEMS
3. Etching
4. Surface micromachining
5. **Bulk micromachining**
6. Molding

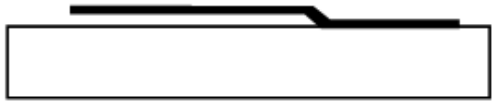
Bulk Micromachining vs Surface Micromachining



Bulk micro-machining

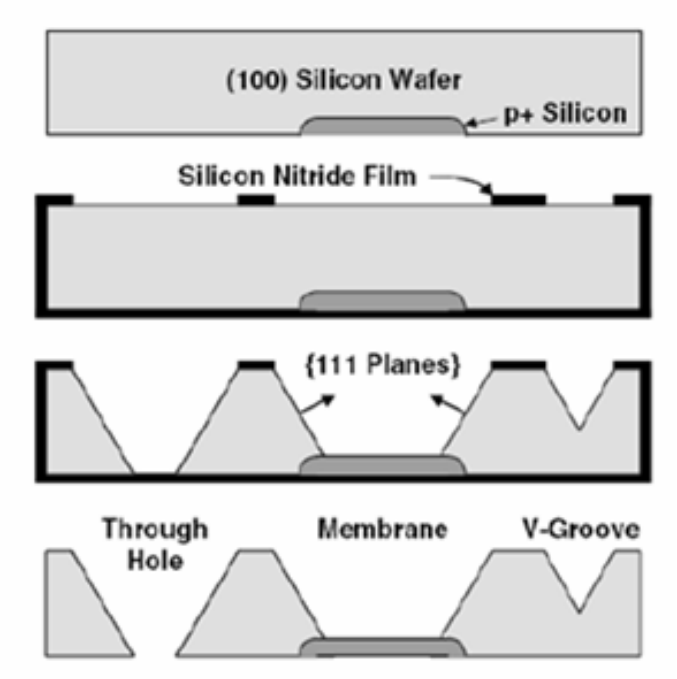


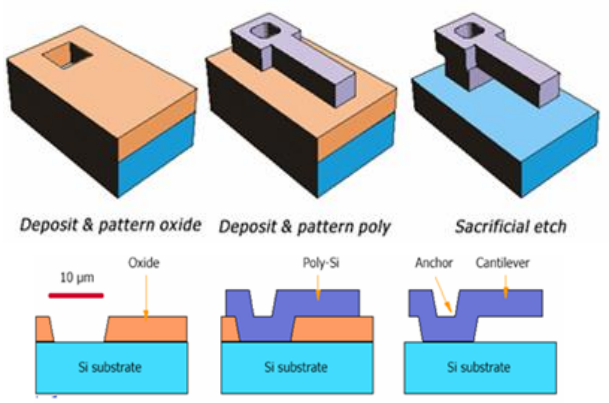
Surface micro-machining



Bulk Micromachining

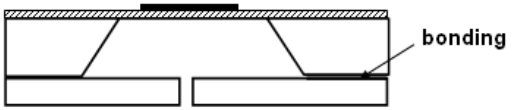
- Selectively remove significant amount of silicon from wafer
- Oxidation of silicon
- Products physically removed from substrate
- Isotropic and anisotropic
- Large structures can be fabricated
- 3D (V-grooves, channels, pits…)
- Compatible with CMOS technology



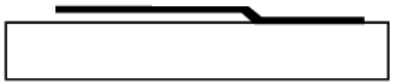


Sandia National Laboratory

Bulk micro-machining

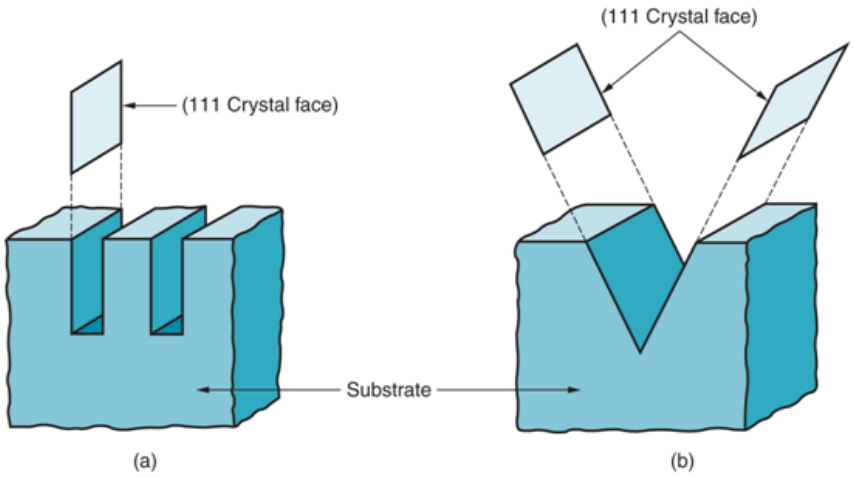


Surface micro-machining



Bulk Micromachining

- Certain etching solutions, such as potassium hydroxide (KOH), have a very low etching rate in the direction of the (111) crystal face. This permits formation of distinct geometric structures with sharp edges in single-crystal Si.
- Bulk micromachining: relatively deep wet etching process on single-crystal silicon substrate
- Surface micromachining: planar structuring of the substrate surface, using much more shallow etching.
- Several structures that can be formed in single-crystal silicon substrate by: (a) (110) silicon and (b) (100) silicon (See Fig. below).



M.P. Groove : Fundamentals of Modern Manufacturing, 4th Edition, John Wiley & Sons, Inc. 2010.

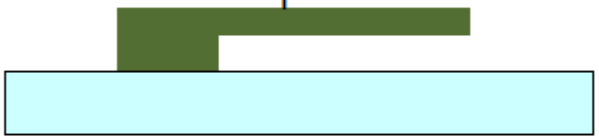
Bulk Micromachining

Etch using a mask

Boron doping using a mask

Flip and bond to a glass

Dissolve undoped silicon in EDP



Boron doped dissolved wafer process (Michigan)

Etch a cavity in a wafer

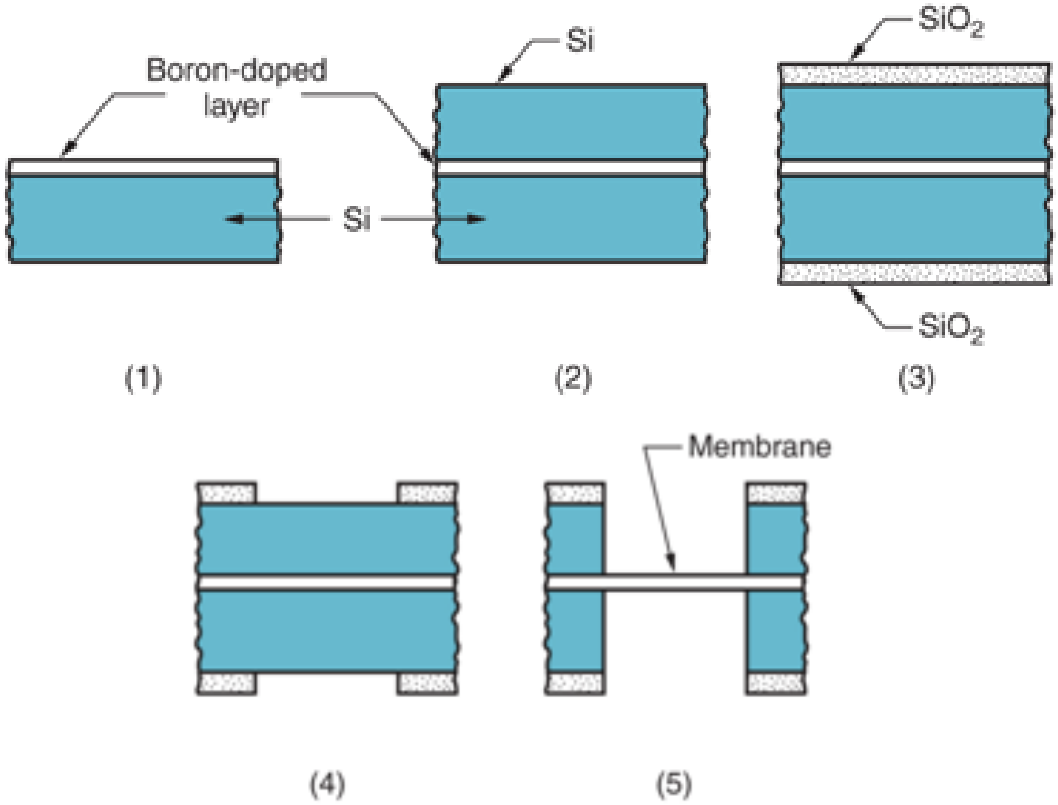
Bond another wafer

Thin down / polish and etch

MIT's wafer bonding process

Bulk Micromachining to Form Thin Membrane

(1) Si substrate is doped with boron, (2) a thick layer of Si is applied on doped layer by epitaxial deposition, (3) both sides are thermally oxidized to form a SiO_2 resist on the surfaces, (4) resist is patterned by lithography, and (5) anisotropic etching removes the Si except in the boron doped layer



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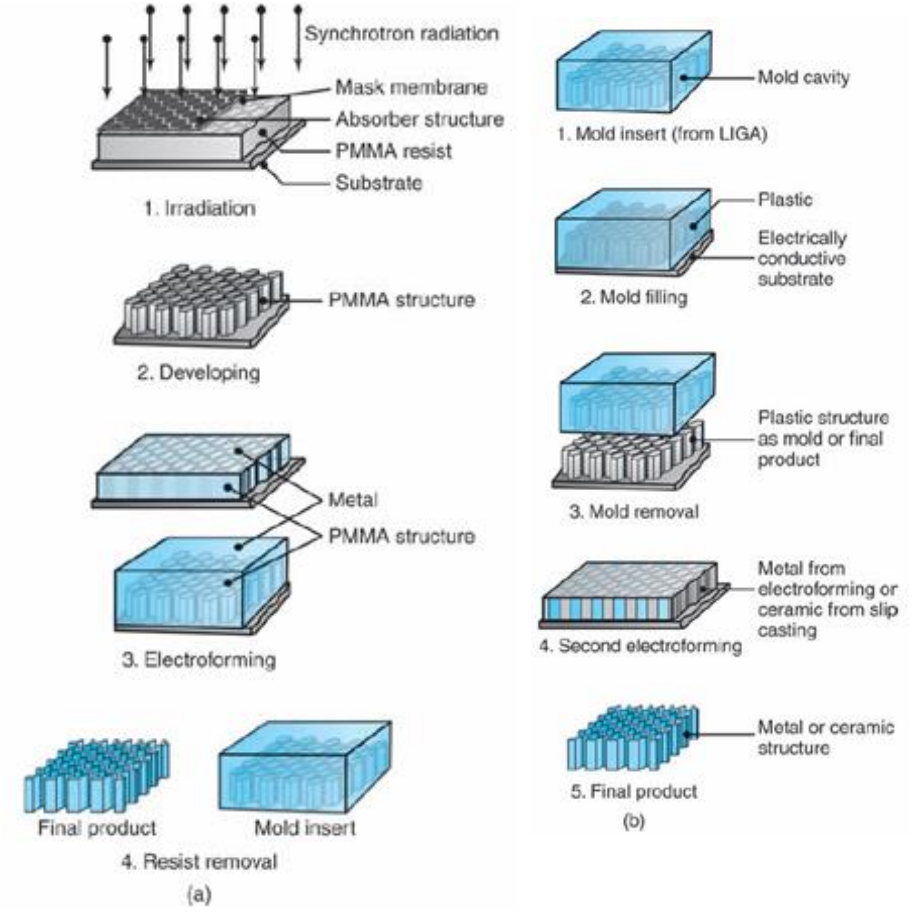
LIGA Process

- A combined processes of X-ray lithography, electrodeposition, and molding. Developed in the early 1990's.
- LIGA consists of the following steps: (i) a thick PMMA (polymethyl methacrylate) of hundreds micrometers is deposited on a preimary substrate; (ii) The PMMA is exposed to X-rays and developed; (iii) Metal is electrodeposited onto the primary substrate; (iv) PMMA Is removed, resulting in a freestanding metal structure and (v) plastic is injection molded into the metal structure.



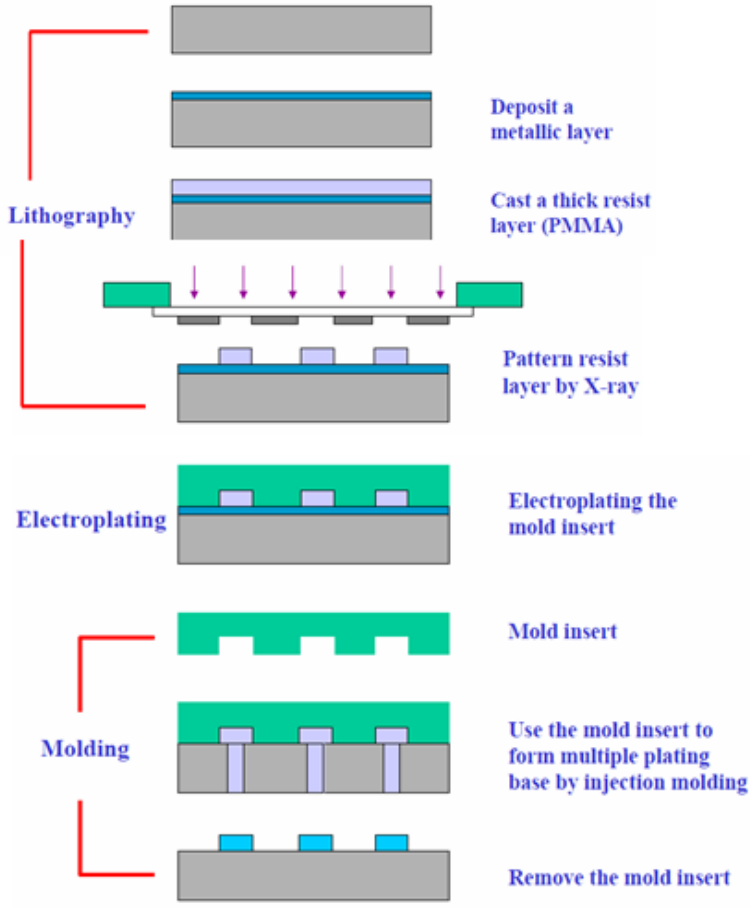
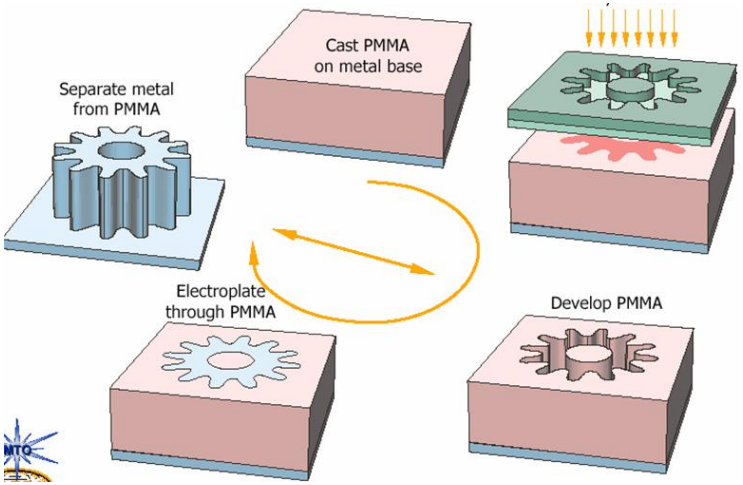


Figure source: J. Bryzek, K. Petersen, and W. McCulley IEEE Spectrum, 1994

- LIGA stands for the German words : Lithographie (in particular X-ray lithography), Galvanoformung (translated electrodeposition or electroforming) , Abformtechnik (plastic molding)

IMM Institut fur Mikrotechnik, Mainz, Germany

LIGA Process



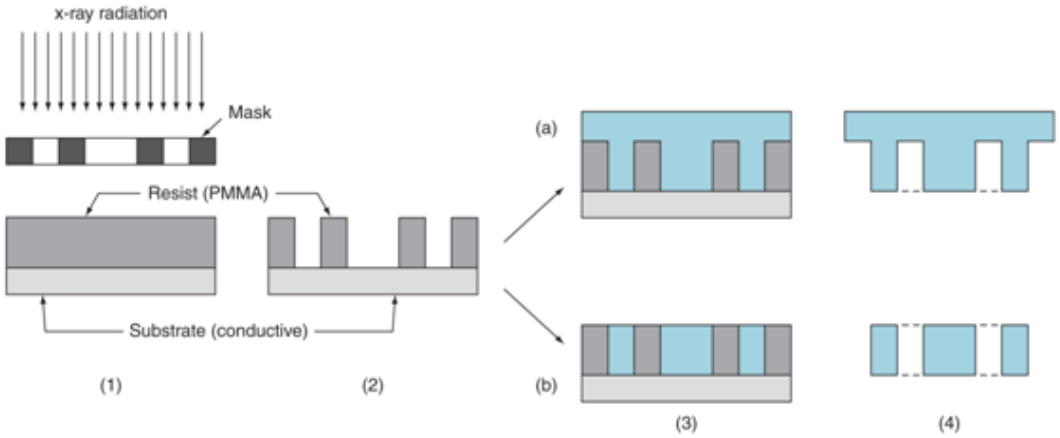
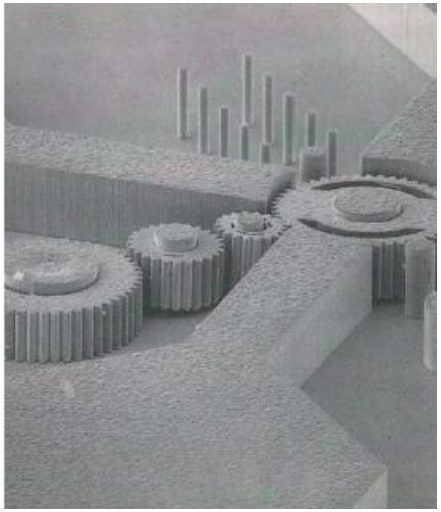


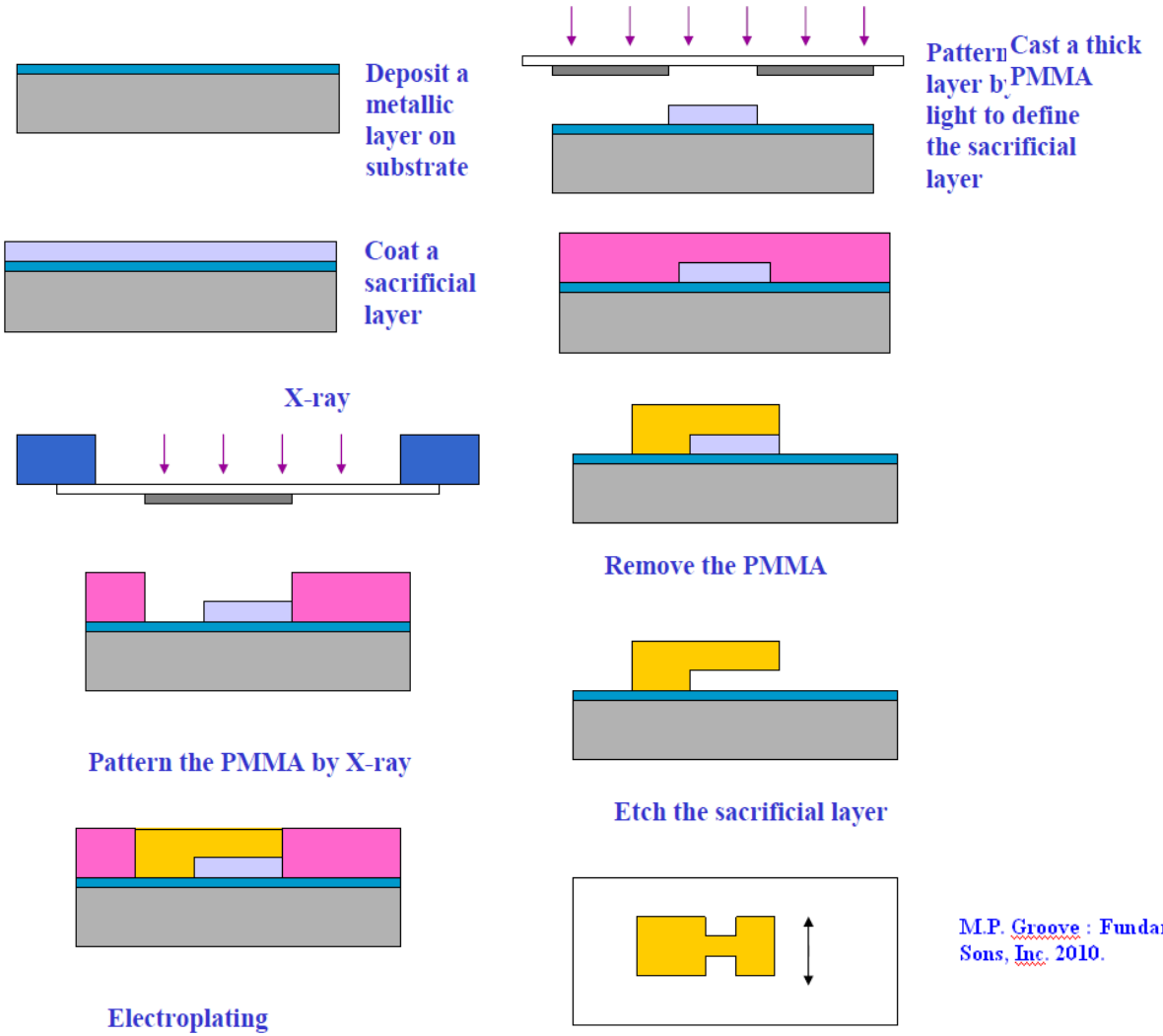
Figure source: J. Bryzek, K. Petersen, and W. McCulley IEEE Spectrum, 1994



M.P. Groove : Fundamentals of Modern Manufacturing, 4th Edition, John Wiley & Sons, Inc. 2010.

SLIGA

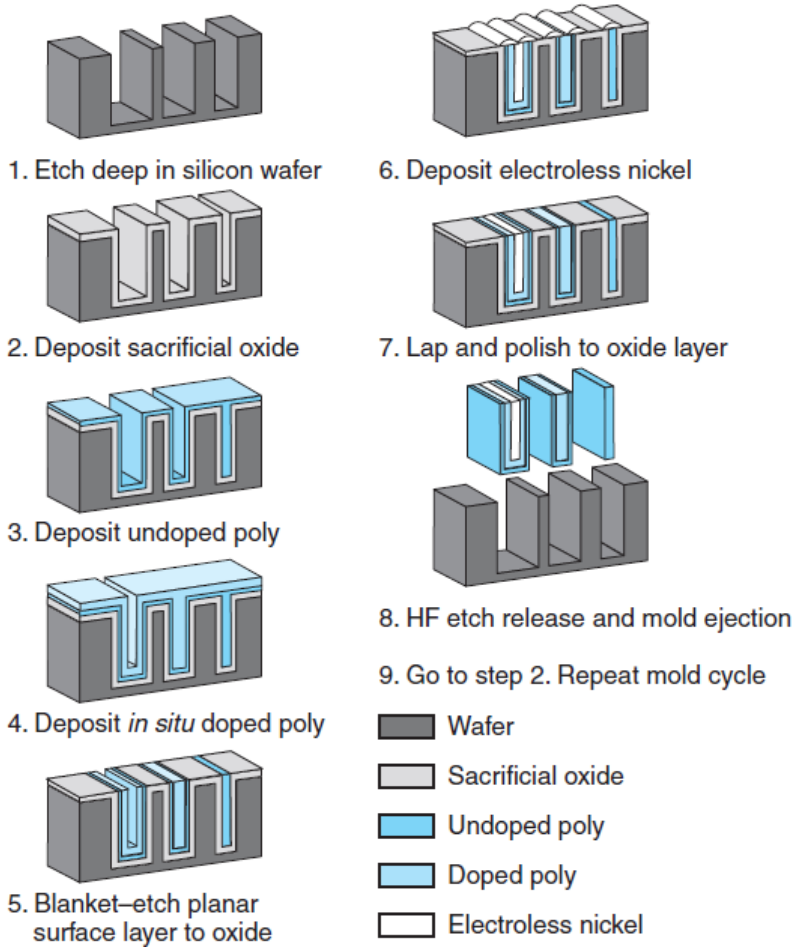
SLIGA – combining the LIGA process with sacrificial layer technique, therefore movable microstructure is available

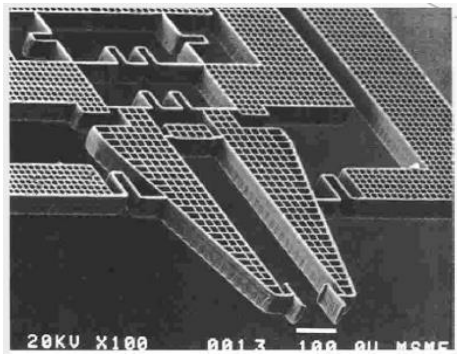


M.P. Groove : Fundamentals of Modern Manufacturing, 4th Edition, John Wiley & Sons, Inc. 2010.

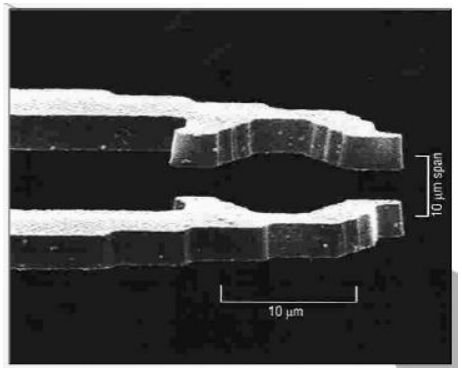
HEXSIL

- HEXIL: combines hexagonal honeycomb structures, silicon micromachining, and thin film deposition.
- A deep trech is first produced in single-crystal silicon by dry etching, followed by shallow wet etching to make the trench walls smoother.
- The depth of the trench is limited to 100 μm. An oxide layer is deposited onto the silicon, followed by an undoped polysilicon for mold filling and shape definition.
- A doped-silicon layer then follows, providing a resistive portion of the device.
- Electroplated or electroless nickel plating is deposited.





HEXIL- Micro-tweezer

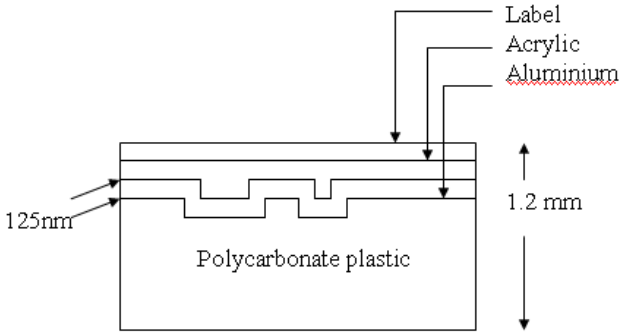


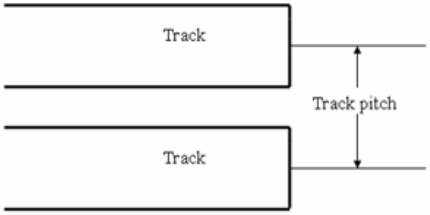
HEXIL- Micro-gripper (Berkeley)

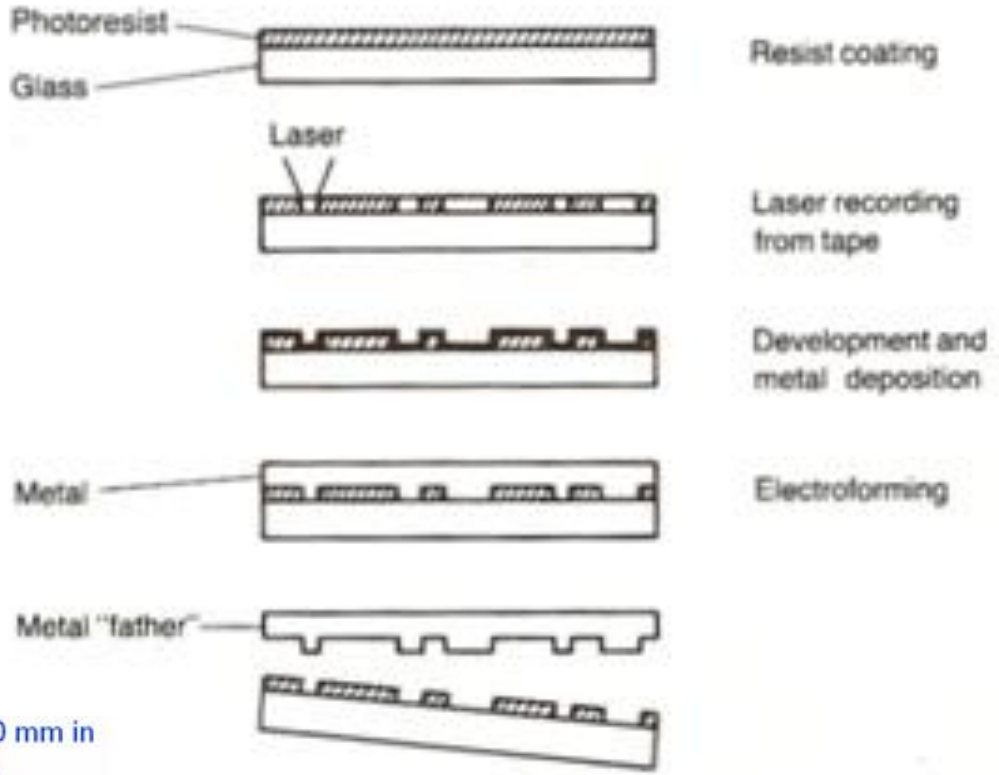
Fabrication of Microelectromechanical Devices and Systems by Kalpakjian

Our MEMS-Related Works

Process of Making CD (Tran et al.)

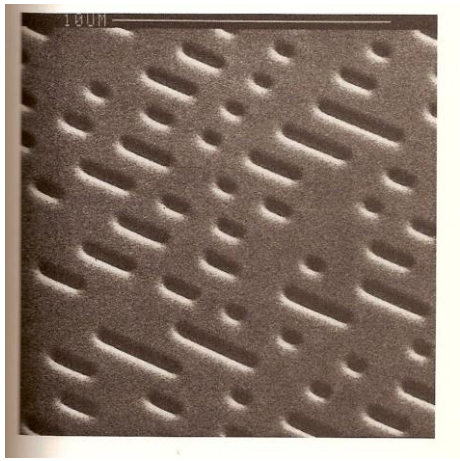






- Glass master disc : begins with a glass plate, 240 mm in diameter, 5.9 cm thick. It is washed , lapped and polished. Photoresist (spinning) is coated following an adhesive (for example, silane coupling agent) . Dropouts were tested with laser. The disc is then stored in an oven for several weeks.
- Photoresist: AZ photoresist iscoated, baked and developed.

Process of Making CD (cont'd)

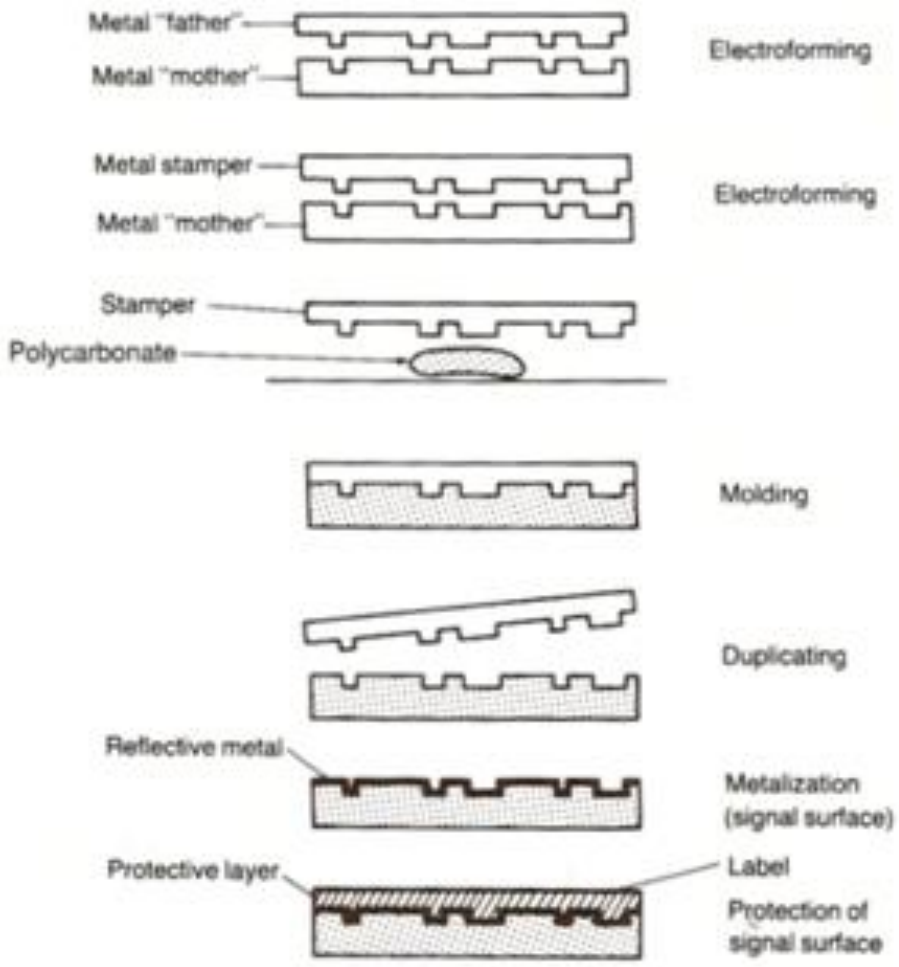


Actual image of lands and pits on CD

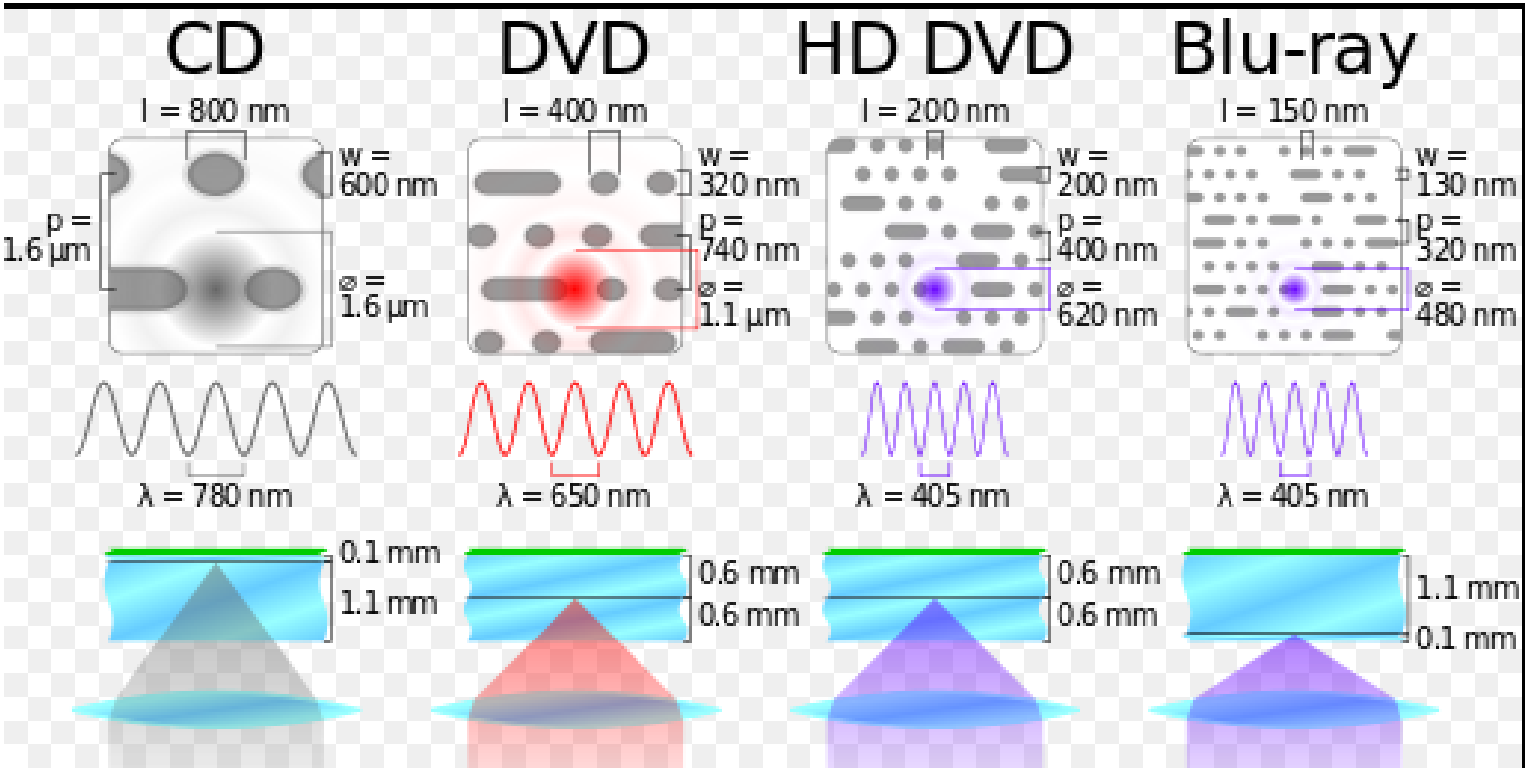
(5,000X Magnification)

- ✓CD has the following dimension: size of data track (track length is about 3.5 miles) : 0.5 μm wide, 1.6 μm center-to-center from one tract to the next.
- ✓Elongated bumps are 0.5 μm wide, a minimum 0.83 μm long and 125 nm high

- Injection molding: molten plastic is injected into a mold cavity; the disc is ready for replication. Polycarbonate is used since it has high transparency, dimensional stability, good impact resistance, good processing characteristics, free of impurities.



Schematic of CD, DVD and Blu-ray

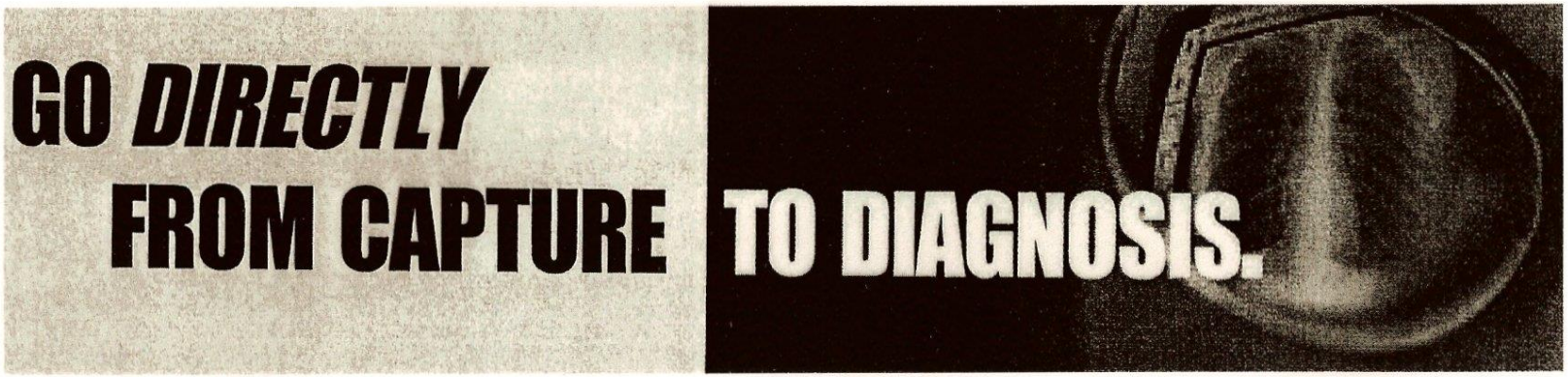


(Google's image)

Density ∝ (NA/λ)²

2nd generation
SD Video
4.7 GB / 8.5 GB
1X: 11 Mb/s
4 Gb/in²
λ = 650 nm
NA = 0.60
0.6 mm substrate

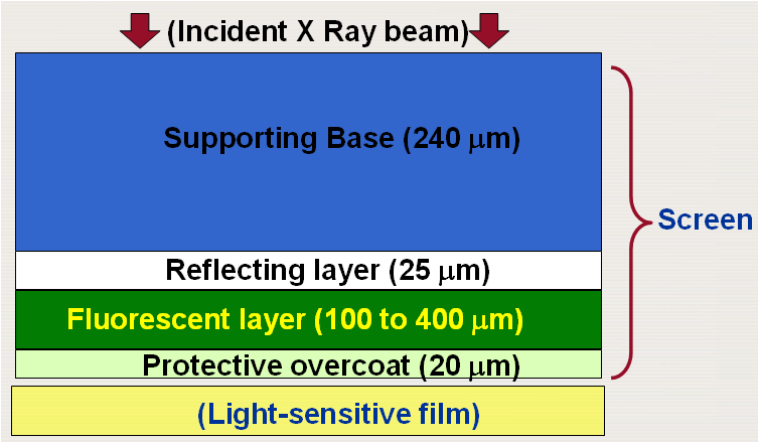
3rd generation
HD Video
25 GB / 50 GB
1X: 36 Mb/s
19 Gb/in²
λ = 405 nm
NA = 0.85
0.1 mm cover

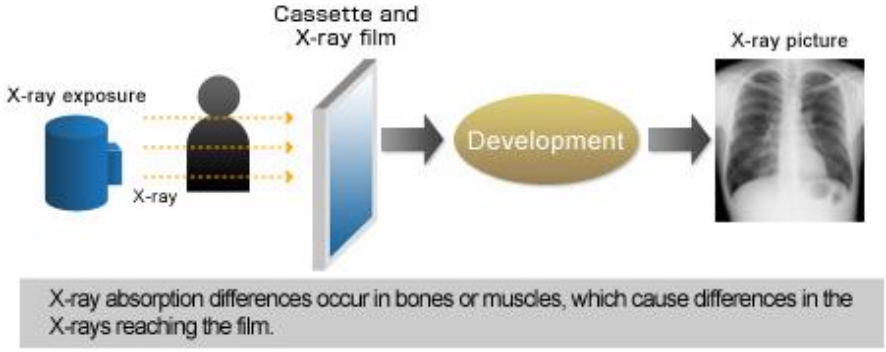


Direct X-Rays Digital Radiography

(Where large area electronics, medical physics and thin film technology cross)

Issues With Analog X-ray Imaging

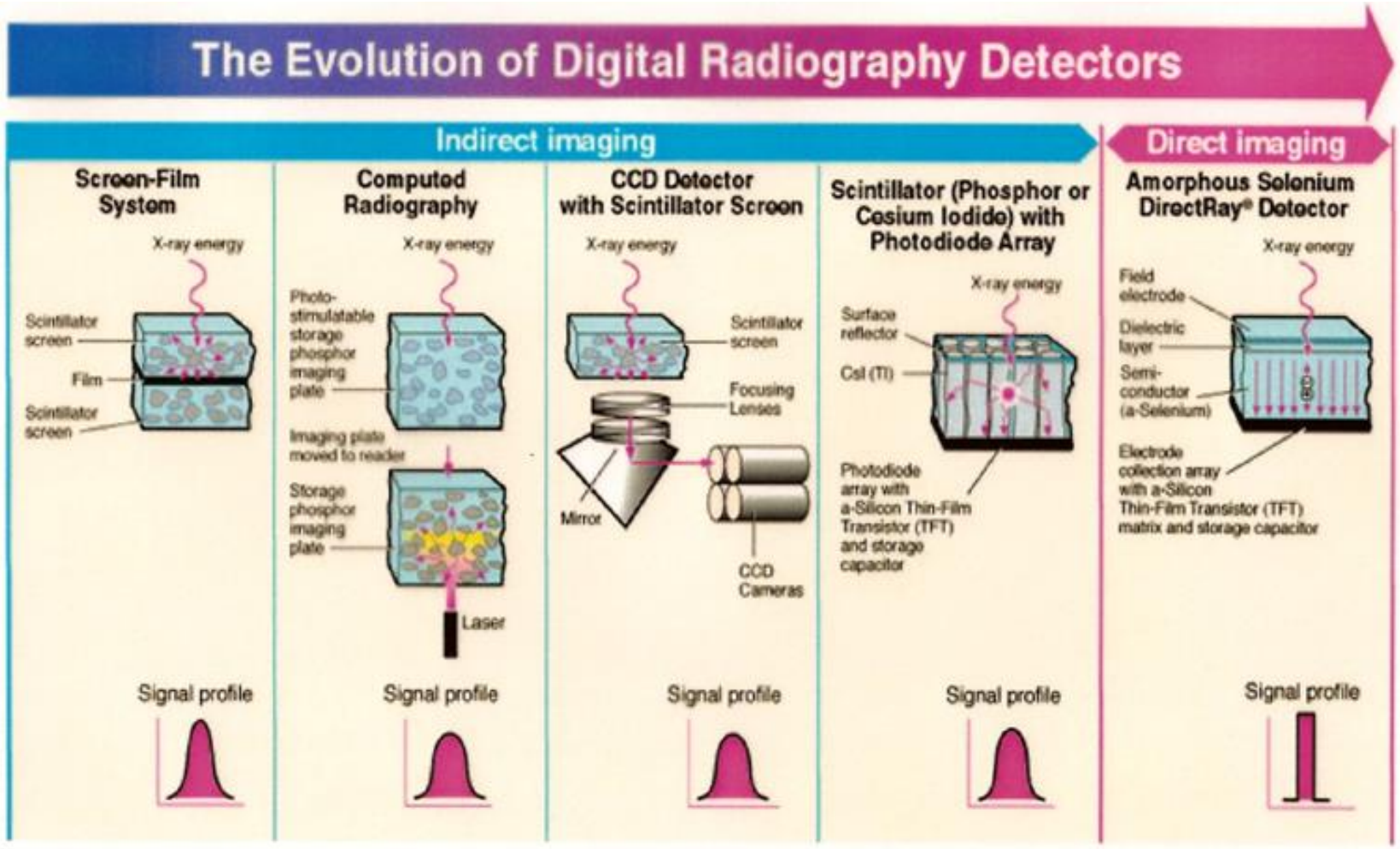




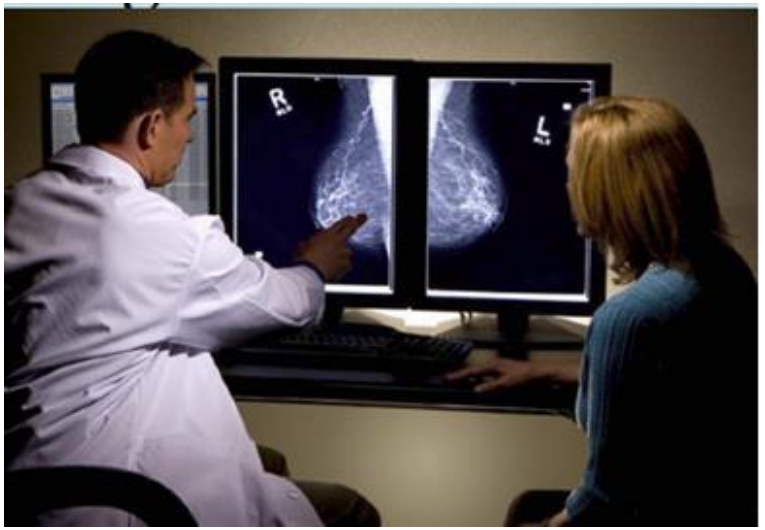
The Challenges

- Improved image quality
- Wider dynamic range
- Reduced exam times
- Image manipulation tools
- Removes film variability
- Eliminates processing
- Minimizes retakes

Digital X-rays Radiography

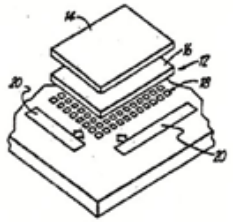


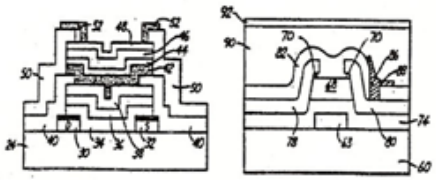
Going DIGITAL!

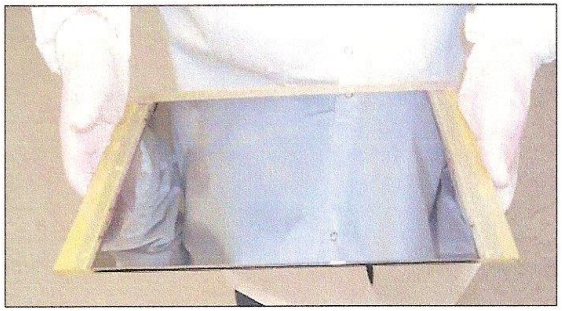


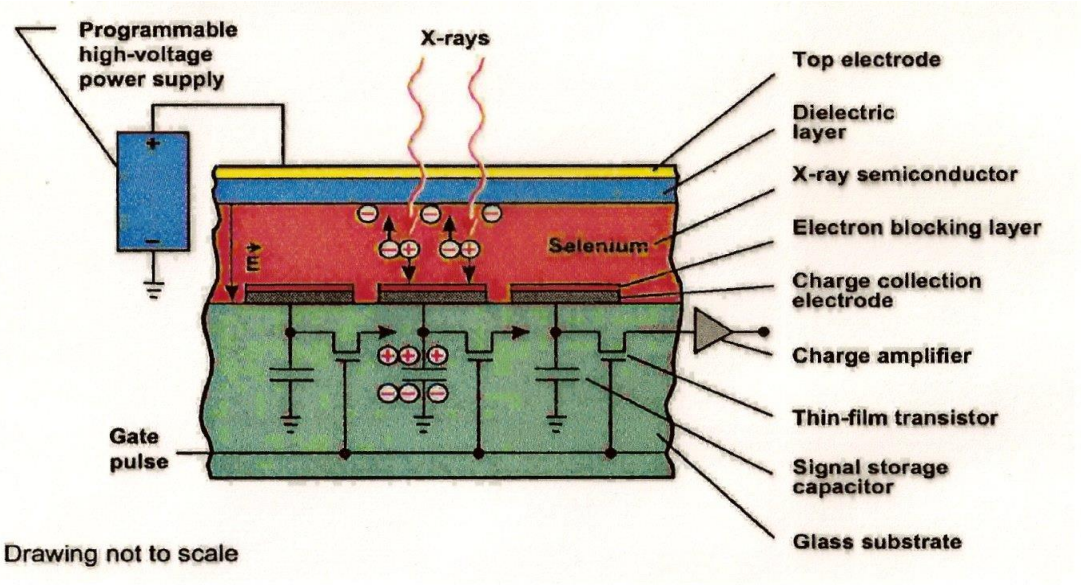
About Our Direct X-rays Detector

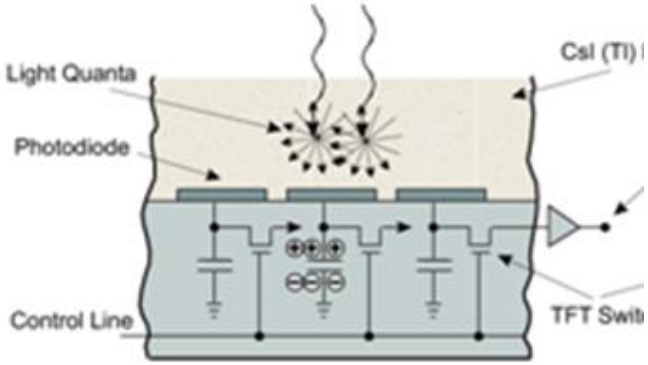
- Nang Tran et al., US patents 5,254,480, 5,235,195, 5,973,311.
  18 : array of thin film transistor, 14 : phosphor , 20 : read-out circuitry, 63 ,78,80: :gate, drain, source.

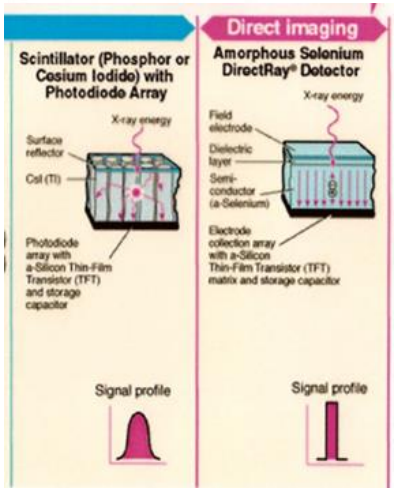




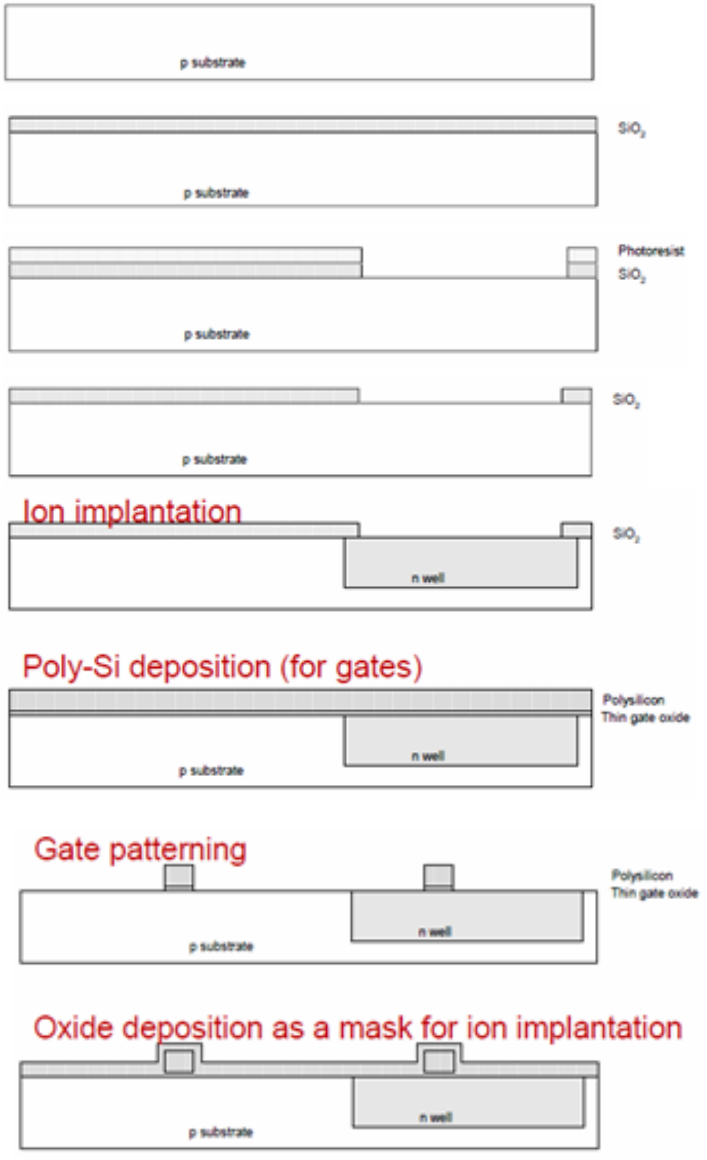


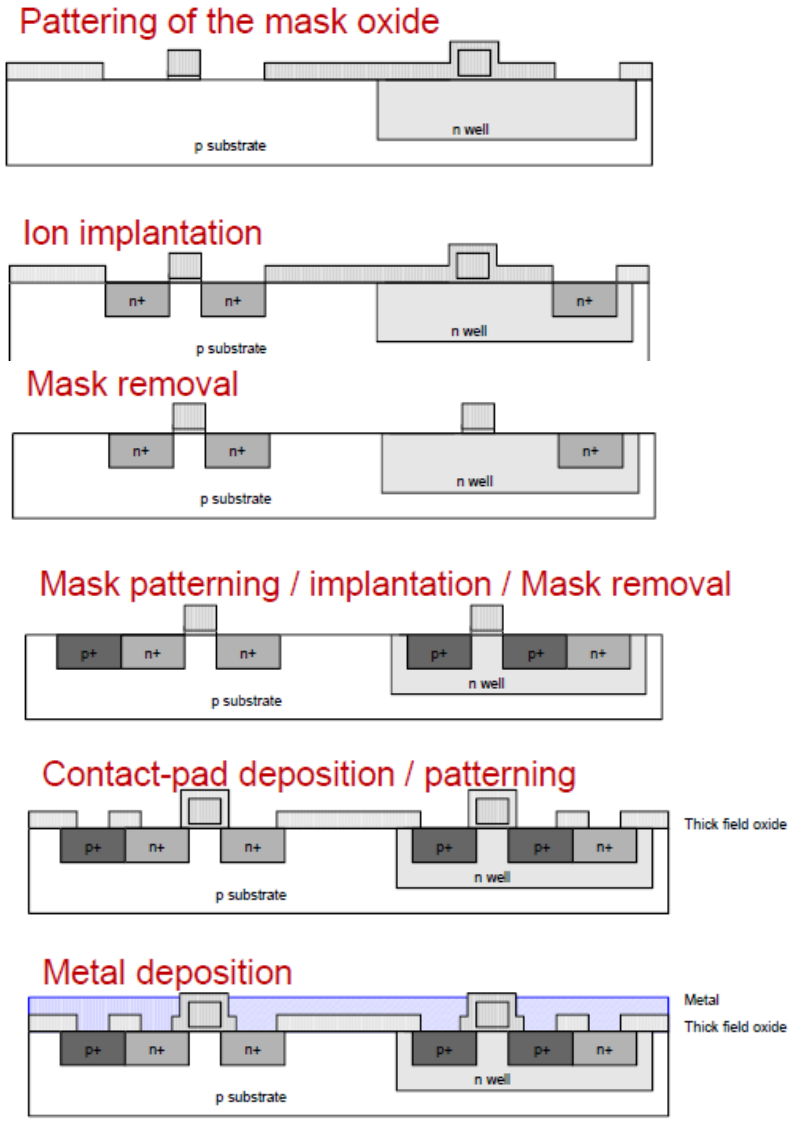






CMOS Fabrication Process





High Temperature Polycrystalline Thin Film Transistor (N. Tran, 1988)

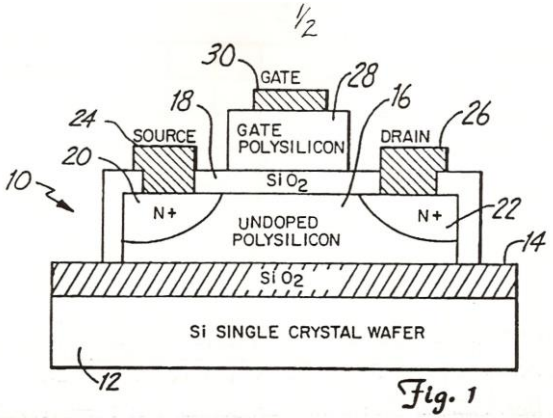


Fig. 1

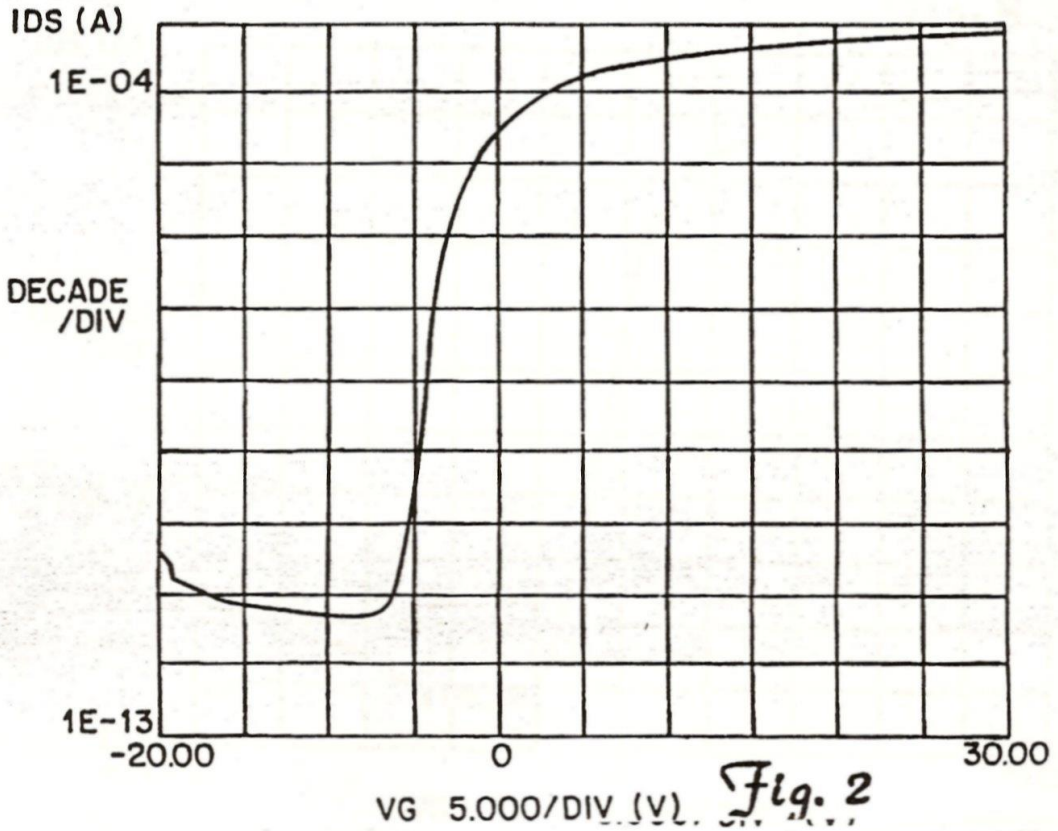
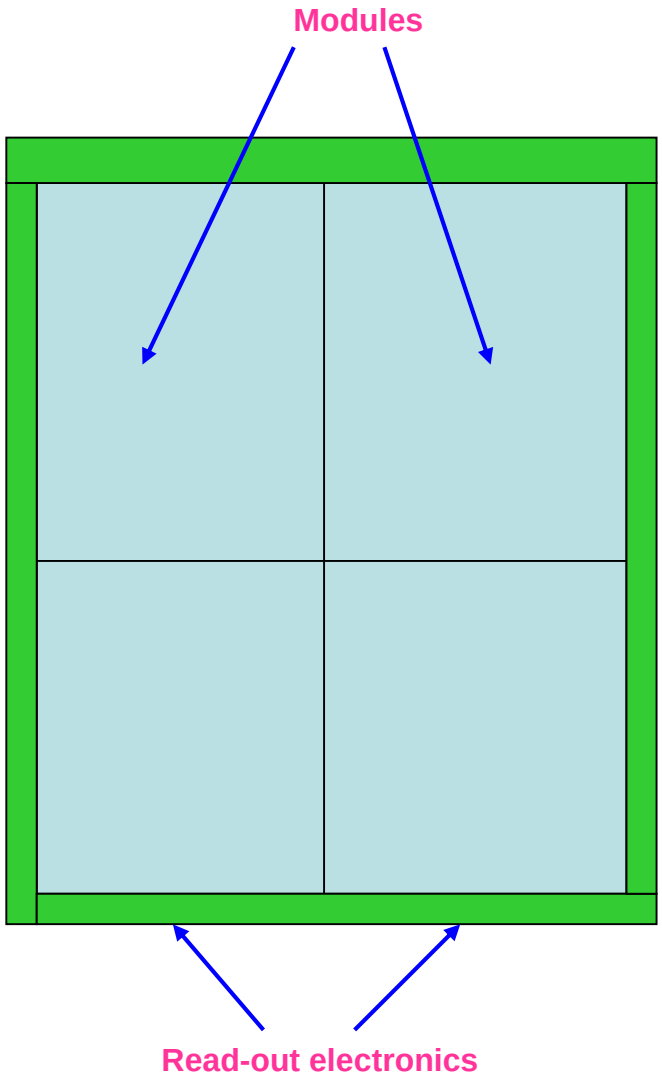
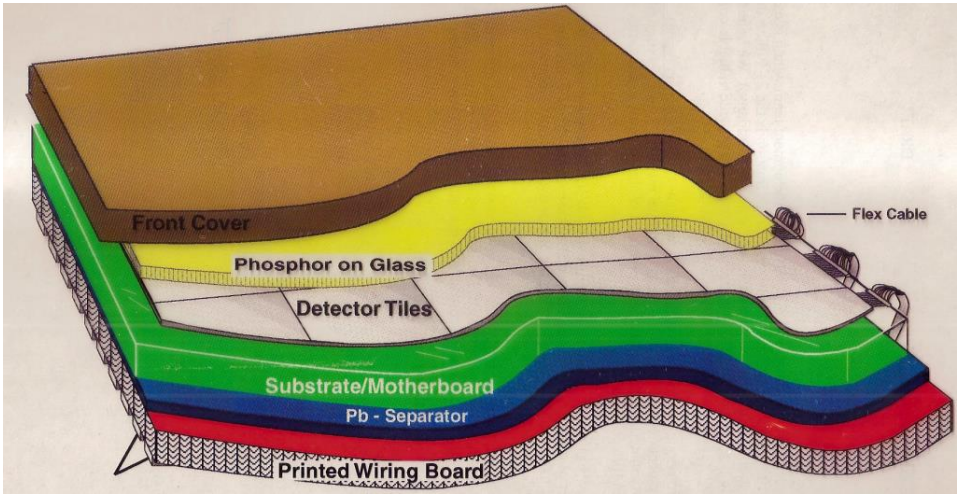


Fig. 2

Tiling Approach

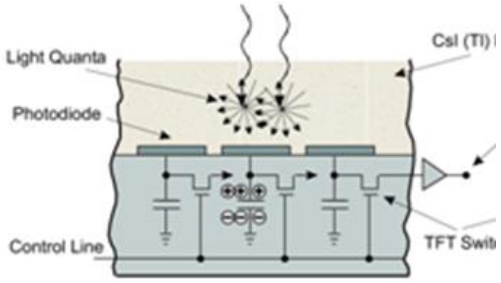


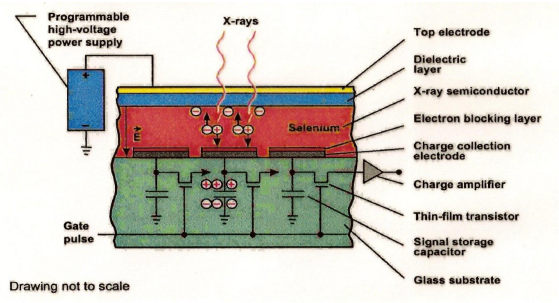


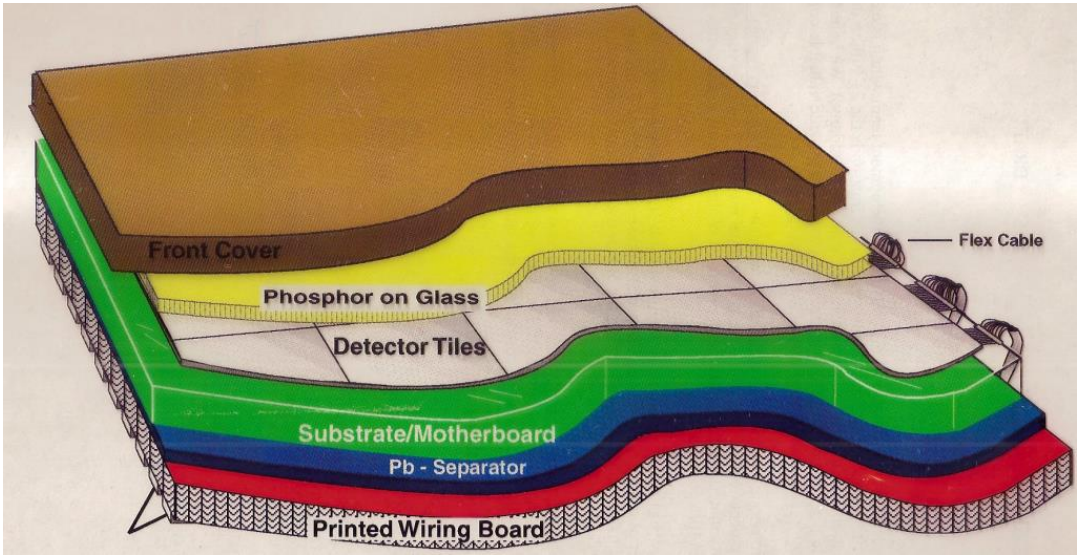
Our proposed c-Si based tiling approach

About Our c-Si Approach

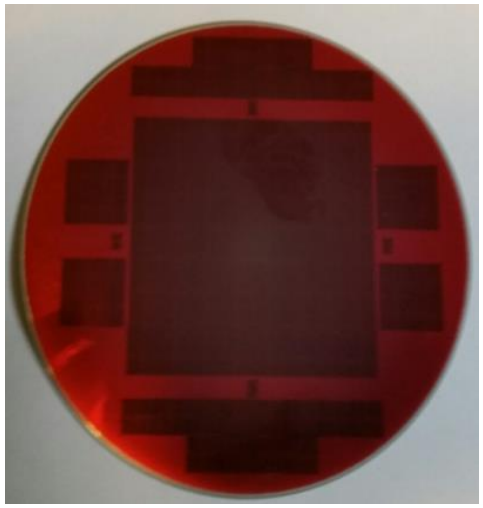
- **Using a proven silicon technology**.
- Less development time. Potentially lower cost.
- High performance single crystal Si. Structured phosphor.
- Smaller tiles mean higher yield
- Ease in maintenance: soldering/desoldering
- Crowdedness and low FF due to busses and circuitry (*wafer thinning*).
- Combining small Si chips without dead space? How to bring out signals from the individual tiles? *(circuitry is distributed throughout the array- four-side- buttable tile)*





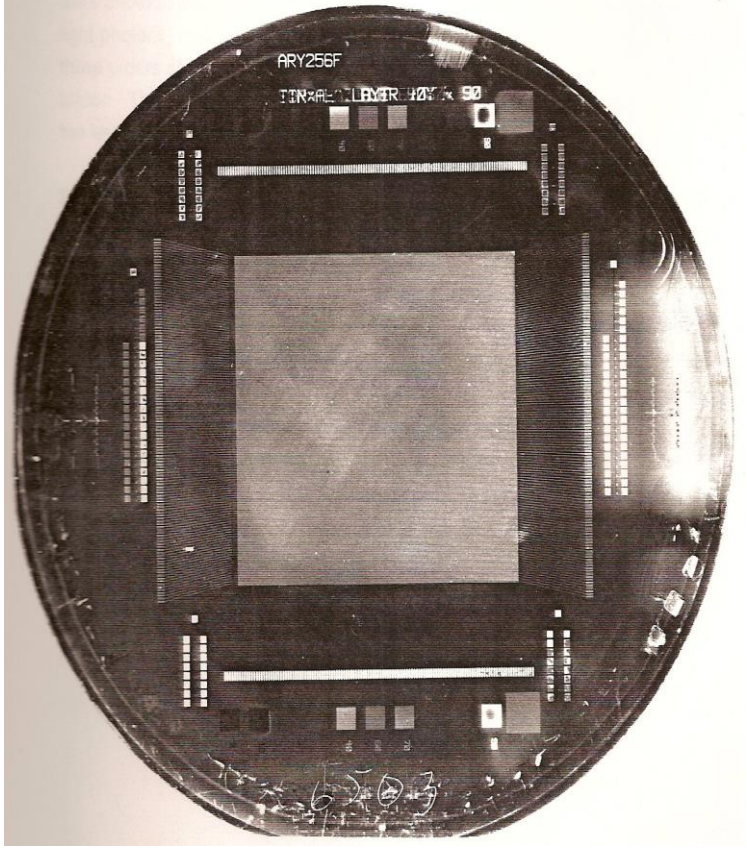


Our Historic Digital X-rays Detector



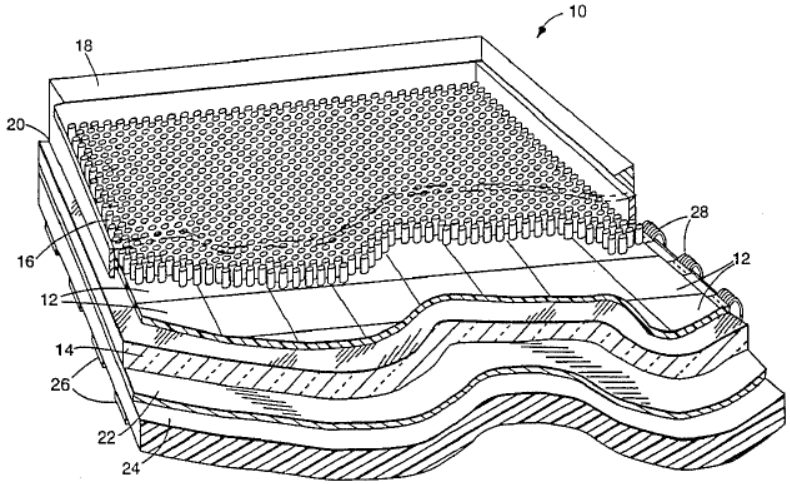
3M

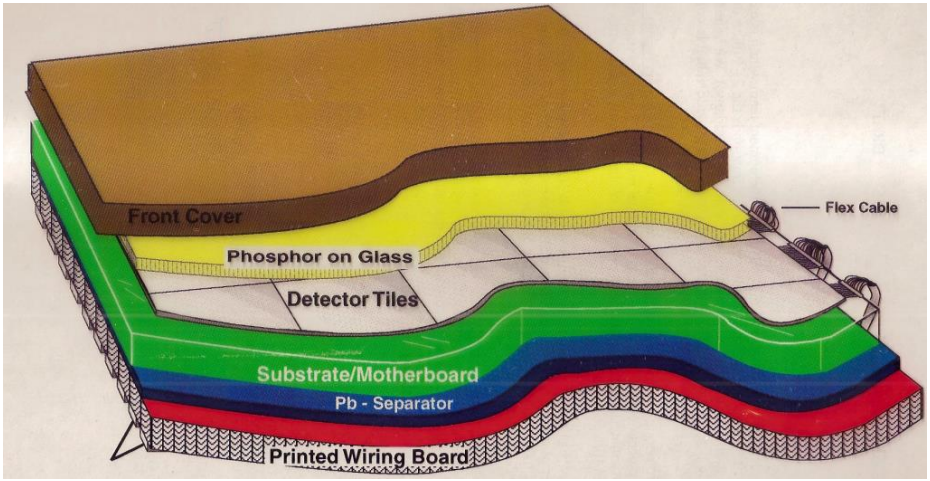
Figure 3. Photograph of 256 x 256-Pixel Solid State Radiation Detector



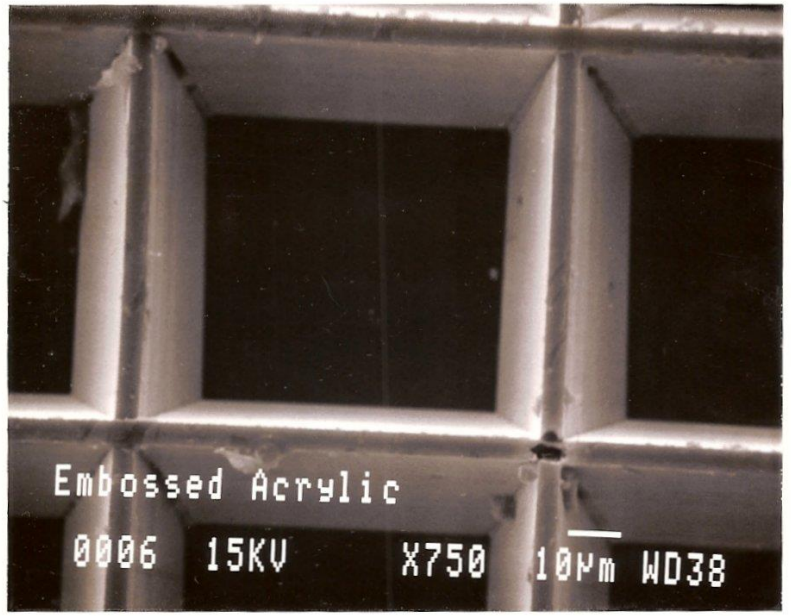
About Our Digital X-rays Detector

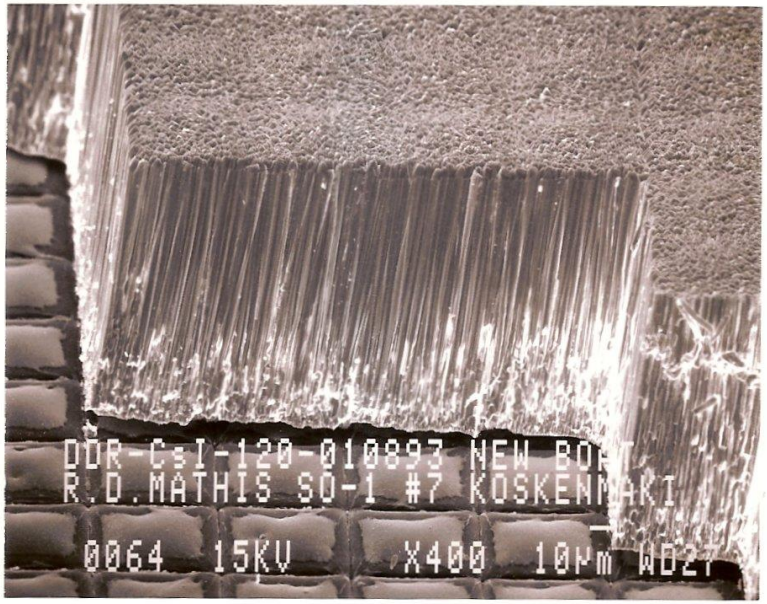
- Using silicon technology.
- Using bulk micromachining (molding) to make structured phosphor
- Thinning silicon wafer.
- Smaller tiles mean higher yield



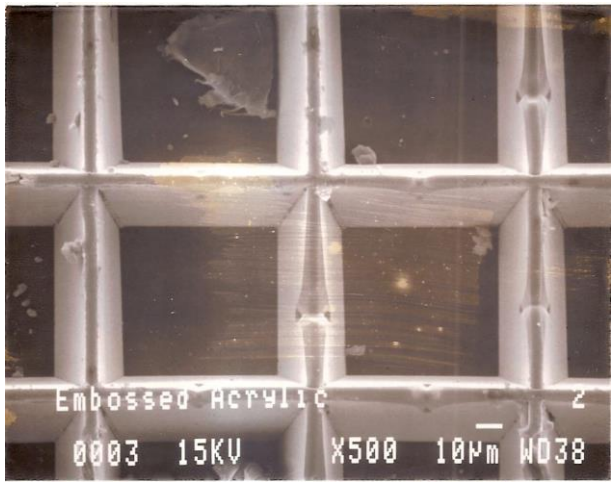


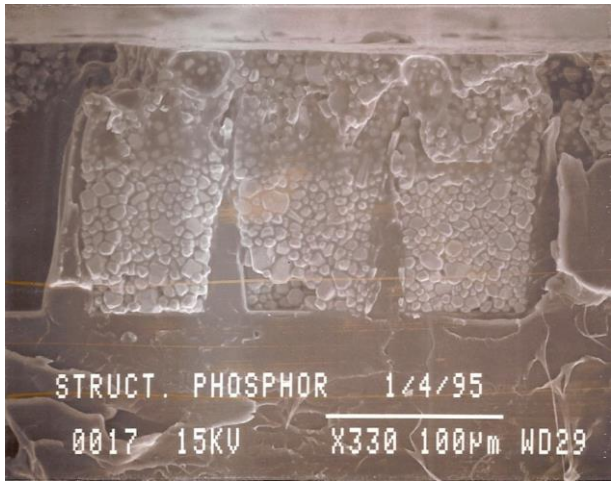
Microreplication/ Microstructures (N.Tran et al.)

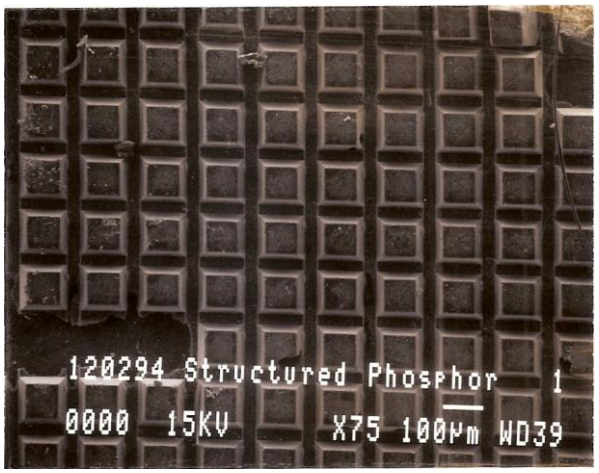


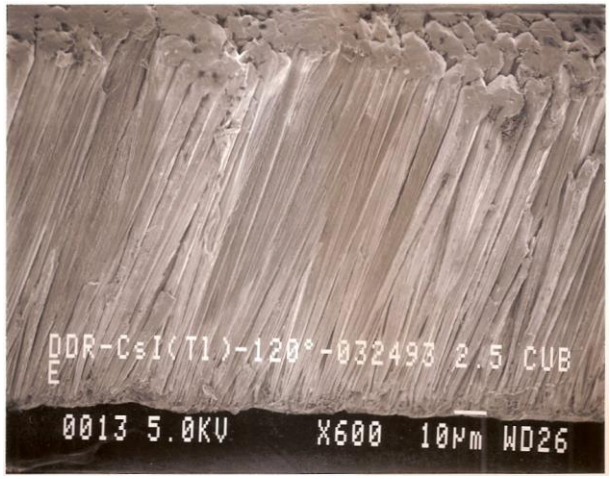


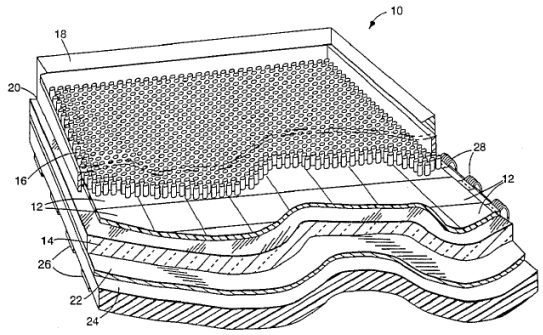
Different Techniques of Fabricating Structured Phosphors





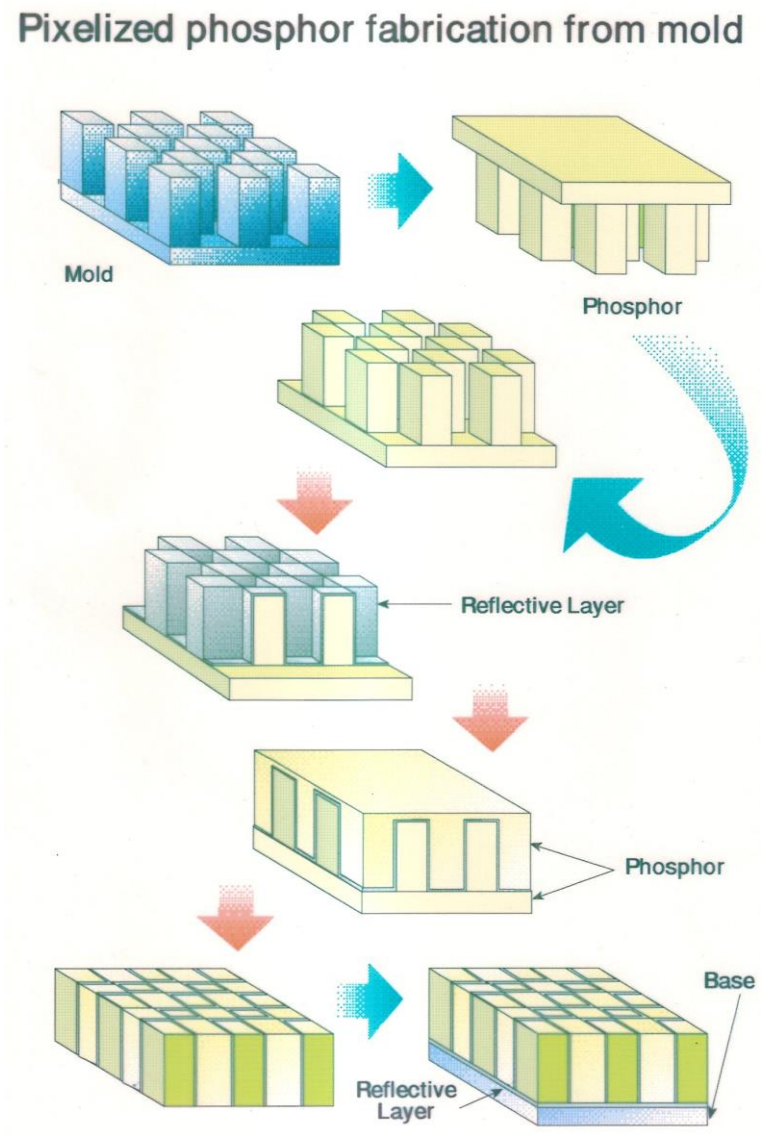


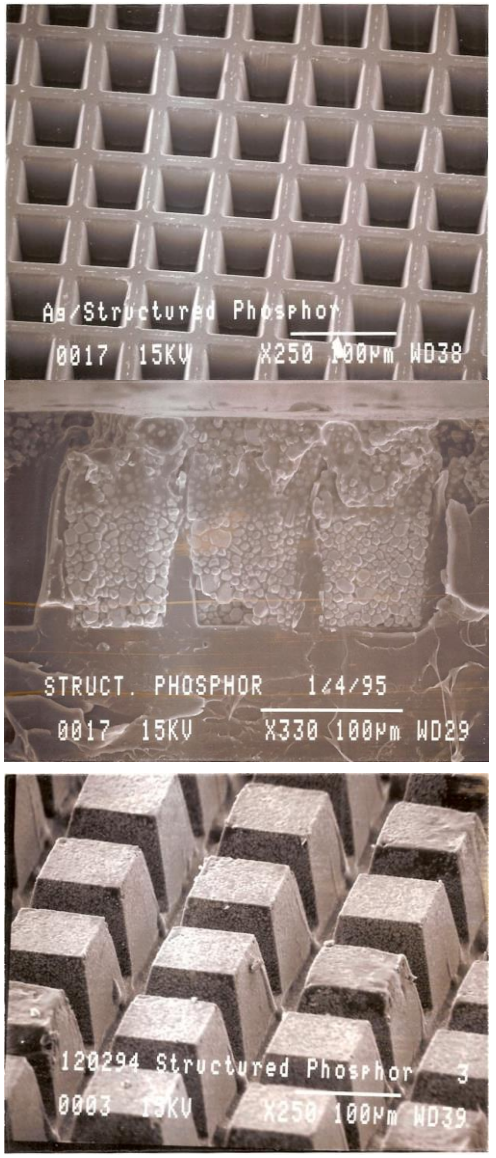




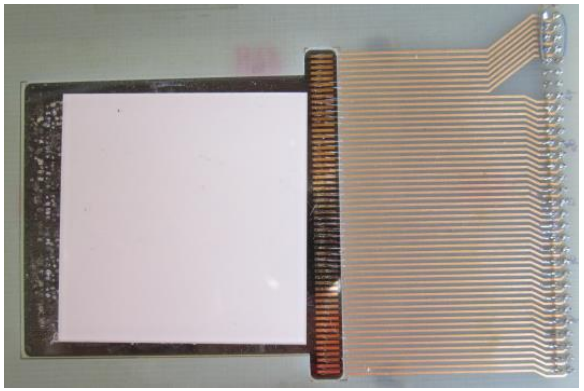
N. Tran et al.

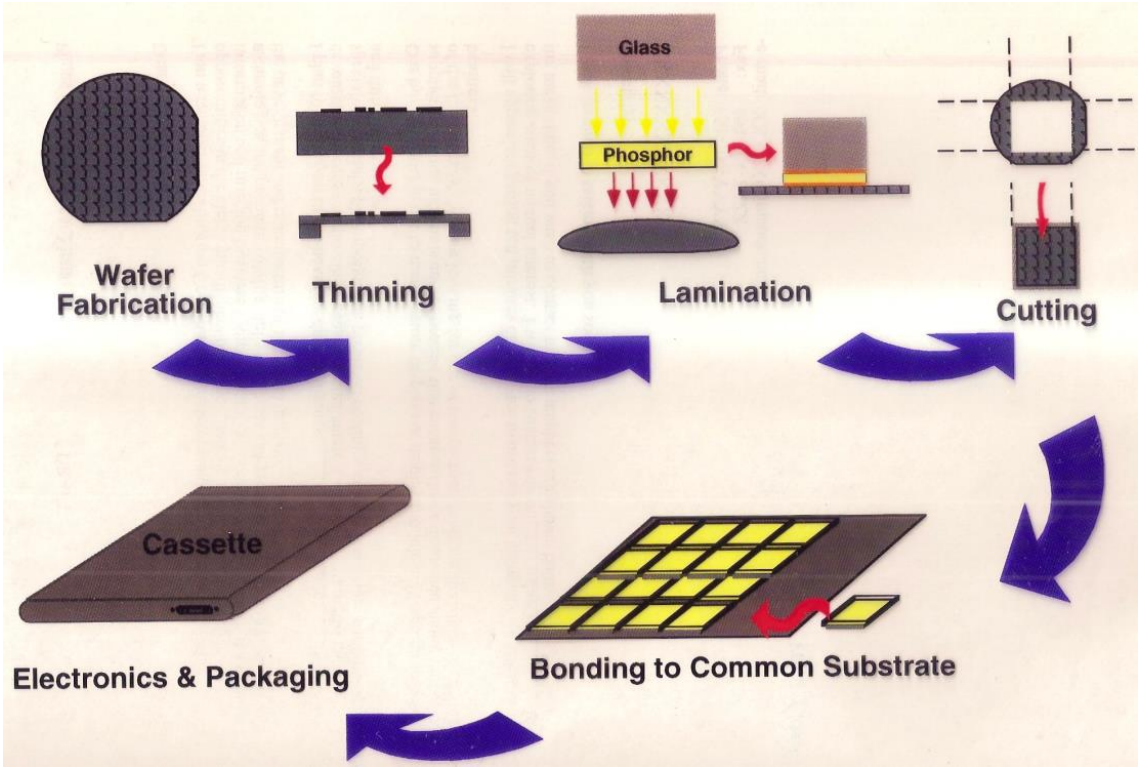
Pixelized Phosphor Fabrication From Mold (N. Tran et al.)

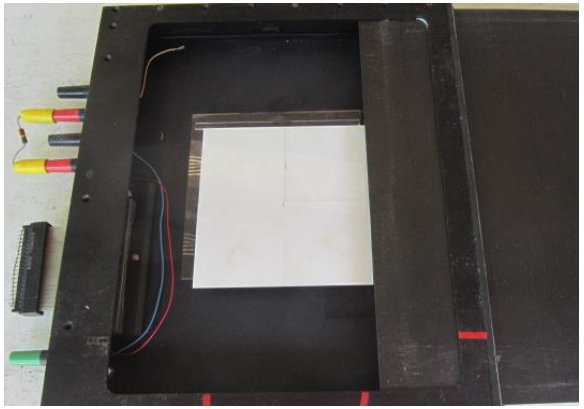


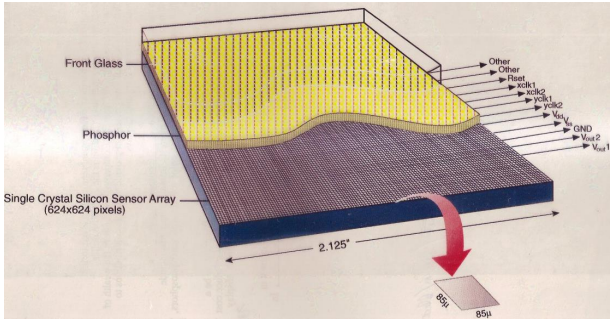


DR Process Overview (N. Tran et al.)

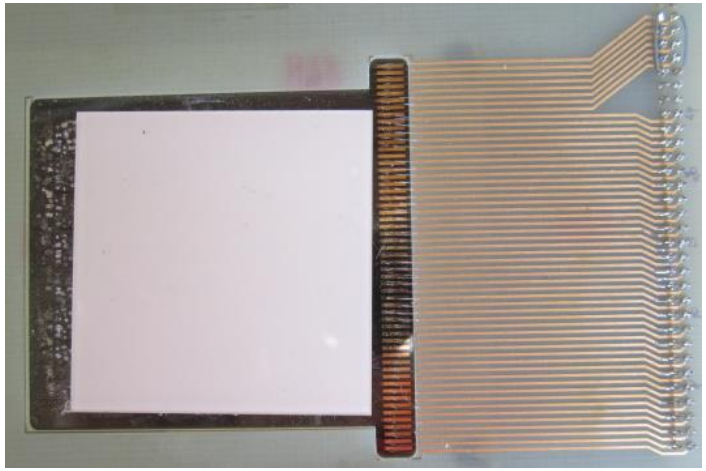


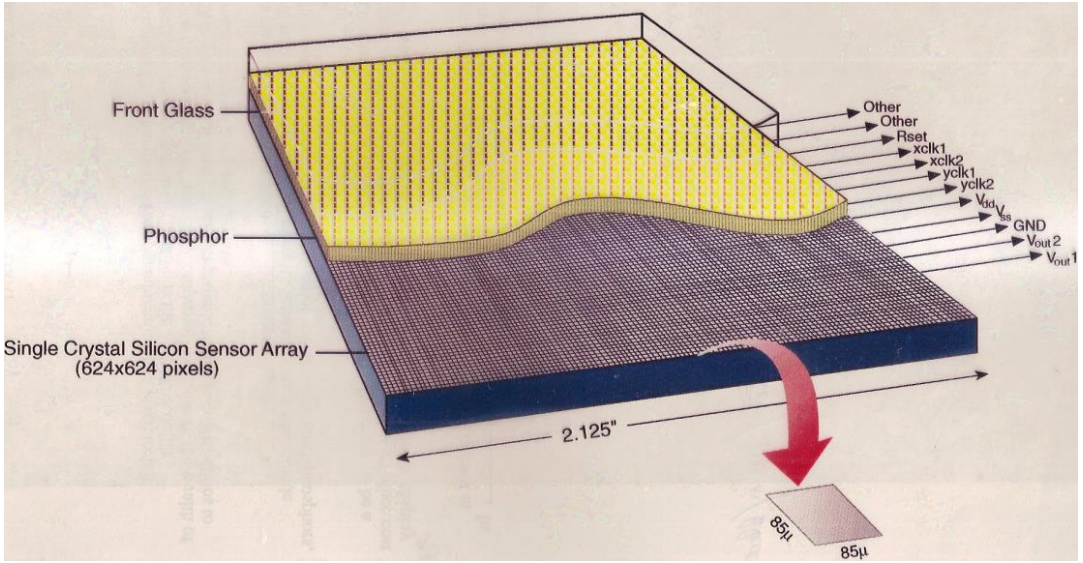


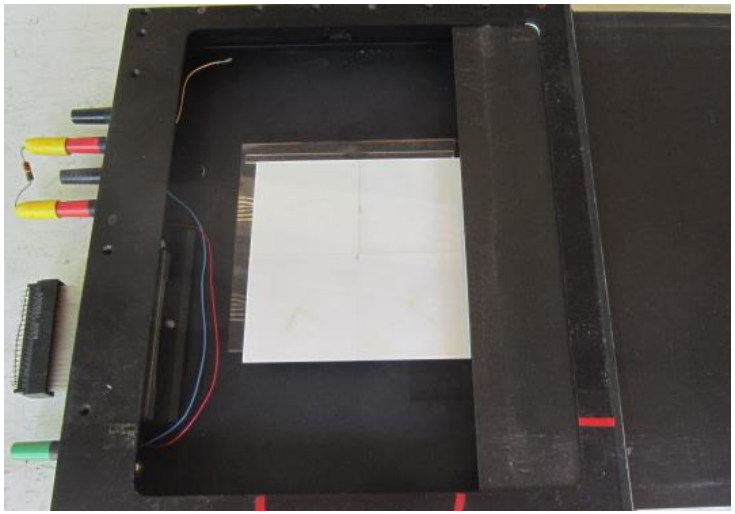


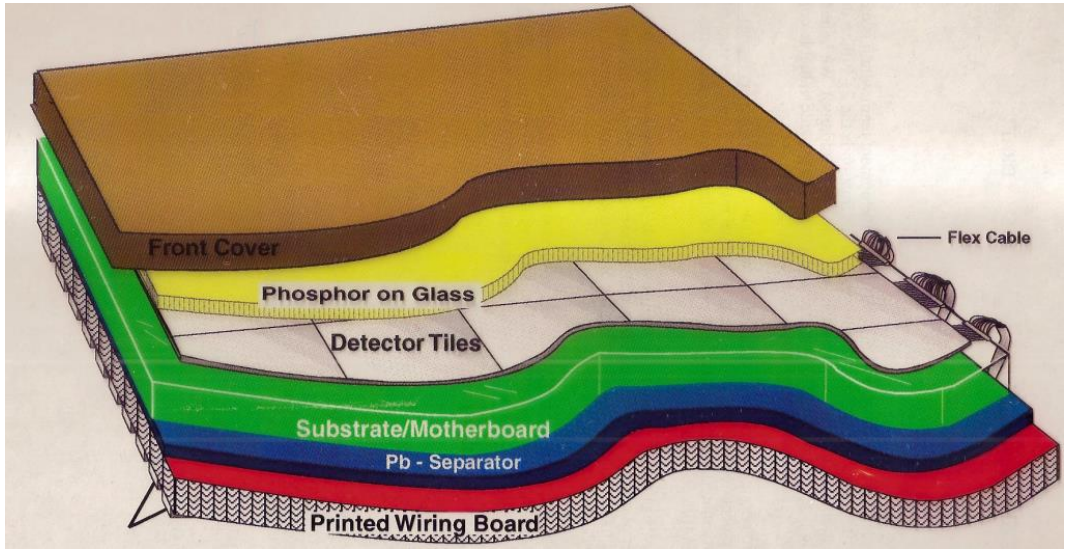


C-Si - based DR Detectors



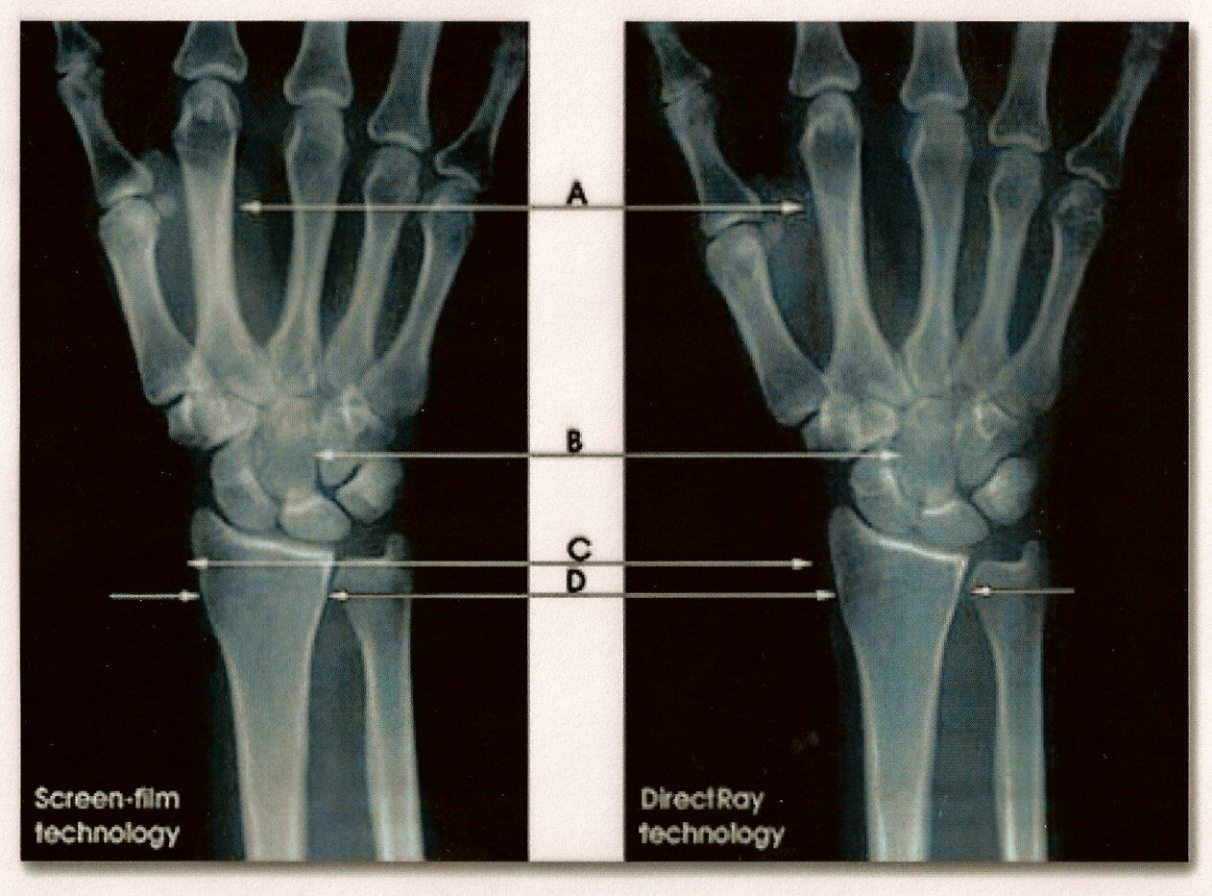






X-rays Imaging of Hands

Conventional film-screen technology vs. Direct digital technology




That's All Folks!

Additional Materials

A micro-diaphragm pressure sensor

(Sugiyama et al.)

Deposit a nitride layer using LPCVD

Etch the nitride layer to leave a square window

Deposit polysilicon using LPCVD

Deposit a thick nitride layer

Deposit polysilicon piezoresistors

Deposit another nitride layer

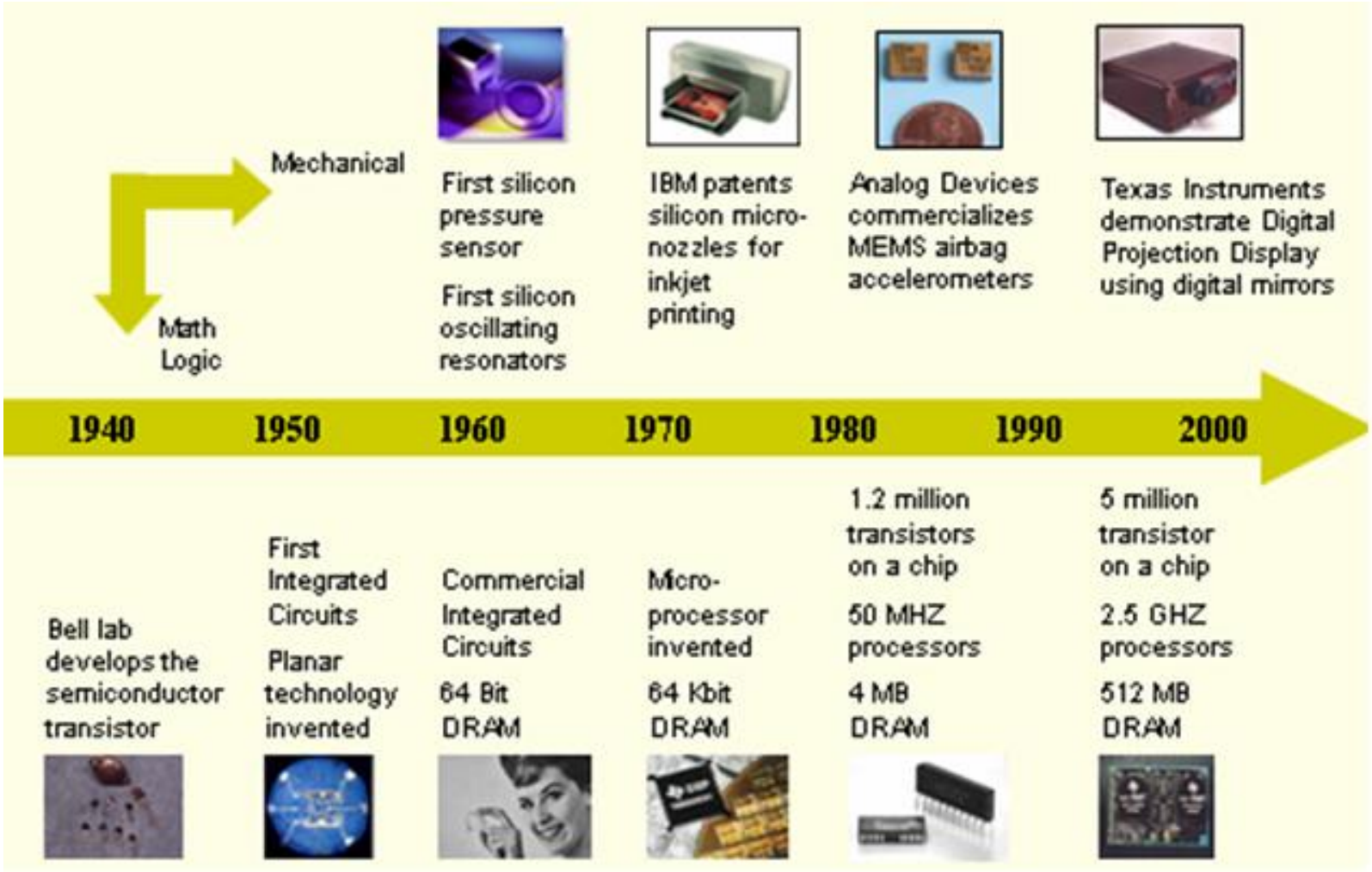
Etch nitride layers

Etch polysilicon and silicon using KOH

Deposit Al using vacuum evaporation and pattern

Seal using a nitride layer using plasma CVD

The Mechanical Face of the Silicon Revolution



Mohammad Kilani